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MODELING AND IMPLEMENTATION OF HIGH PERFORMANCE MEMS-BASED OSCILLATOR

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MODÉLISATION ET IMPLÉMENTATION D'OSCILLATEUR MEMS À HAUTES PERFORMANCES

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LIST OF ABBREVIATIONS

AGC	Automatic Gain Control
AHDL	Analog Hardware Description Language
BW	Bandwidth
C-C	Clamped-Clamped
CMFB	Common-mode Feedback
CMOS	Complementary Metal-Oxide Semiconductor
CSFB	common Source Feedback
DC	Direct Current
DOF	Degree-Of-Freedom
EOM	Equation Of Motion
FOM	Figure-of-merit
IC	Integrated Circuit
MEMS	Microelectromechanical System
PCB	Printed Circuit Board
ppm	part per million
QFN	Quad-Flat No-leads
RGC	Regulated Cascode
RMS	Root Mean Square
SEM	Scanning Electron Microscope
SOI	Silicon-On-Insulator
SSF	Super Source Follower
TIA	Transimpedance Amplifier
TSMC	Taiwan Semiconductor Manufacturing Company

VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer

LIST OF SYMBOLS

γ	Noise coefficient
κ	Amplitude-frequency (A-f) coefficient
$\overline{i_{n,in}^2}$	Mean squared input referred noise current
ϕ	Phase shift
C_P	Parasitic capacitance
F	Noise factor
g_{d0}	Zero-bias drain conductance of MOS transistor
g_{ds}	Conductance of MOS transistor
g_m	Transconductance of MOS transistor
k	Boltzmann's constant
P_{DC}	Power consumption
Q	Quality factor
R_{in}	Input impedance
r_o	Output resistance of MOS transistor
R_{out}	Output impedance
T	Absolute temperature
Z_T	Transimpedance gain

ABSTRACT

The interest in tiny timing applications has been increased over the past decade with regard to an integrated reference oscillator which can offer same performance as oscillators based on quartz crystal. Microelectromechanical systems (MEMS) are considered as a good candidate that can have advantages regarding size scaling and integration with other fabrication processes at lower cost.

The objective of this dissertation is to realize a high performance fully differential transimpedance amplifier (TIA) for a highly integrated reference oscillator. The purpose of this circuit will be of sustaining oscillation from a MEMS resonator in closed-loop. This thesis covers non-linearity effects of MEMS resonator in which a Verilog-A model of clamped-clamped (C-C) beam resonator is presented so that electrical and mechanical non-linearities are exposed with this model. A MEMS-based oscillator is implemented by incorporating a transimpedance amplifier designed in 0.13 μm with the Verilog-A model. The phase noise performance dependance on the resonator non-linear effects and its polarisation voltage are illustrated through simulations. Simulation results confirm that careful design must be applied when MEMS resonators are utilised in order to ensure that non-linearities and biasing do not significantly deteriorate oscillator performance.

In addition, two designs of fully differential transimpedance amplifier are designed in order to meet the specifications of MEMS oscillators based on piezoelectric and capacitive resonators, respectively, in terms of quality factor and insertion loss. The TIAs are designed in 65 nm CMOS process to take advantages of larger gain-bandwidth product wither lower power consumption which it can be offered by this technology, and thus to offset the resonator losses and to ensure a small phase shift so that high oscillation frequencies (larger than 20 MHz) can be attained. Furthermore, gain and bandwidth can be adjustable separately and input and output impedances reduction methods are applied to avoid loading the resonator's quality factor at a low power-consumption cost.

The first design uses a regulated cascode (RGC) topology as an input stage to benefit of higher gain and lower input impedance. Thus, the TIA can provide enough gain and bandwidth to sustain oscillation and compensate the losses of the capacitive resonators. The proposed TIA consumes 1.4 mA from 1-V supply. The measured mid-band transimpedance gain is 80 dBΩ and the TIA features an adjustable bandwidth with a maximum bandwidth of 214 MHz. The measure input-referred current noise of the TIA

at mid-band is below 4 pA/$\sqrt{\text{Hz}}$. The TIA is integrated with the MEMS piezoelectric disk resonator and the oscillator performance in terms of phase noise and frequency stability is reported. The measure phase noise in air and under vacuum is about -104 dBc/Hz and -116 dBc/Hz, respectively, at 1-kHz offset, while the phase noise floor reaches -130 dBc/Hz. The measured short-term stability of the MEMS-based oscillator is ± 0.38 ppm.

Finally, the second design presents a novel fully differential transimpedance amplifier, using the advantages of the regulated cascode (RGC) and common source active feedback topologies, suitable for oscillators based on piezoelectric resonators. The TIA consumes 0.9 mA from 1-V supply. The measured mid-band transimpedance gain is 98 dBΩ and the TIA features an adjustable bandwidth with a maximum bandwidth of 142 MHz. The measure input-referred current noise of the TIA at mid-band is below 15 pA/$\sqrt{\text{Hz}}$. The measure phase noise of the oscillator based on Lamé-mode MEMS resonator is about -120 dBc/Hz at 1-kHz offset under vacuum, while the phase noise floor reaches -127 dBc/Hz. The measured short-term stability of the MEMS-based oscillator is ± 0.25 ppm.

Keywords: Transimpedance amplifier, Microelectromechanical system, Oscillator, Capacitive resonator, Piezoelectric resonator.

RÉSUMÉ

Au cours de la dernière décennie, les recherches portant sur les applications à base de référence temporelle ont montré un intérêt ce qui concerne l'oscillateur de référence intégré qui peut offrir les mêmes performances que les oscillateurs à base de cristal de quartz. Les microsystèmes électromécaniques (MEMS) sont considérés comme un candidat idéal qui peut avoir des avantages concernant la réduction de taille et l'intégration avec d'autres processus de fabrication à moindre coût.

L'objectif est de réaliser un amplificateur à transimpédance (TIA) entièrement différentiel à haute performance pour un oscillateur de référence intégré. Le but de ce circuit sera de maintenir l'oscillation d'un résonateur MEMS en boucle fermée. Ce mémoire couvre les effets non linéaires du résonateur MEMS à partir d'un modèle en langage Verilog-A d'une poutre biencastrée. Ceci permet de modéliser les effets de non-linéarité électriques et mécaniques. Un oscillateur basé sur le modèle Verilog-A du résonateur est ainsi implémenté avec un amplificateur à transimpédance conçu en 0.13 μm. La dépendance de la performance du bruit de phase sur les effets non linéaires du résonateur et sa tension de polarisation est illustrée par des simulations. Les résultats de la simulation confirment qu'une conception soigneuse doit être appliquée lorsque les résonateurs MEMS sont utilisés afin de s'assurer que les non-linéarités et les tensions de polarisation ne détériorent pas considérablement les performances des oscillateurs.

En outre, deux modèles d'amplificateur à transimpédance totalement différentiel sont conçus pour répondre aux spécifications des oscillateurs MEMS à base de résonateurs piézoélectriques et capacitifs, respectivement, en matière de facteur de qualité et de perte d'insertion. Les amplificateurs sont conçus dans un processus CMOS 65 nm pour profiter des avantages en matière de larges gain et bande passante avec la moindre consommation de puissance offerts par cette technologie, par conséquent, compenser les pertes du résonateur et pour assurer un petit déphasage afin que des fréquences d'oscillation élevées (supérieures à 20 MHz) puissent être atteintes. De plus, le gain et la bande passante peuvent être réglables séparément et des méthodes de réduction des impédances d'entrée et de sortie sont appliquées pour éviter de charger le facteur de qualité du résonateur à faible coût de consommation.

Le premier design utilise une topologie de cascode régulé (RGC) comme étage d'entrée pour bénéficier d'un gain plus élevé et d'une impédance d'entrée inférieure. Ainsi, l'amplificateur peut fournir suffisamment de gain et de bande passante pour maintenir

l'oscillation et compenser les pertes des résonateurs capacitifs. Le TIA proposé consomme 1.4 mA à partir d'une alimentation de 1 V. Le gain en transimpédance maximal mesuré est de 80 dBΩ et le TIA dispose d'une bande passante réglable avec une bande passante maximale de 214 MHz. La mesure du bruit en courant à l'entrée est inférieure à 4 pA/$\sqrt{\text{Hz}}$. Le TIA est intégré au résonateur piézoélectrique à disque et la performance de l'oscillateur en fonction de bruit de phase et la stabilité de la fréquence a été présentée. La mesure de bruit de phase dans l'air et sous vide est d'environ -104 dBc/Hz et -116 dBc/Hz, respectivement, à un décalage de 1 kHz, tandis que le bruit de phase de fond atteint -130 dBc/Hz. La stabilité mesurée à court terme de l'oscillateur est $\pm$ 0.38 ppm.

Finalement, le deuxième design présente un nouvel amplificateur à transimpédance entièrement différentiel, conçu aux oscillateurs à base de résonateurs piézoélectriques, et ceci en utilisant les avantages des topologies de cascode régulé (RGC) et de source commune en rétroaction active L'amplificateur consomme 0.9 mA à partir d'une alimentation de 1 V. Le gain maximal en transimpédance mesuré est de 98 dBΩ et le TIA dispose d'une bande passante réglable avec une bande passante maximale de 142 MHz. La mesure du bruit en courant à l'entrée est inférieure à 15 pA/$\sqrt{\text{Hz}}$. Le bruit de phase de l'oscillateur mesuré est d'environ -120 dBc/Hz à décalage de 1 kHz sous vide, tandis que le bruit de phase de fond atteint -127 dBc/Hz. La stabilité mesurée à court terme de l'oscillateur basé sur MEMS est de $\pm$0.25 ppm.

Mots-clés : Amplificateur à transimpédance, Microsystème électromécanique, Oscillateur, Résonateur électrostatique, Résonateur piezoélectrique.

INTRODUCTION

Many electronic devices found in today's markets, such as transceivers for data transfer, storage devices and portable electronics rely on timing references to deliver the performance expected from them. One of the essential components in these devices is the quartz crystal, which acts as the master time reference. Several advantages have allowed the quartz crystal to be an excellent choice by the industry for frequency synthesis applications. Quality factor, frequency stability and its performance in terms of phase noise are the main advantages of crystal oscillators. However, crystal oscillators are characterized by having a relatively large size, and are difficult to tightly integrate with other manufacturing technologies, making their cost and footprint relatively large. Several studies over the past decade have shown that oscillators based on micro-electromechanical (MEM) resonators make them excellent candidates to replace crystal-based resonators in timing applications. In comparison to quartz oscillators, MEMS oscillators that are 20% smaller have been commercialized (SiTime Corporation, 2017). Also, several works have developed integration processes of MEM resonators with CMOS technology (Baltes et al., 2002), enabling a potential for further size and cost reductions.

Micromachined resonators can be operated through two main widespread actuation mechanisms: piezoelectric or capacitive. Piezoelectric actuation generally provides high electromechanical transduction efficiencies and low signal transmission losses, resulting in low motional resistances, which is very advantageous as it simplifies the design constraints of the associated electronic circuitry and results in lower power consumption. Also, piezoelectric devices do not require any DC voltage for operation.

However, piezoelectric devices generally suffer from lower quality factors (Hung & Nguyen, 2011; Schneider & Nguyen, 2014; Zuo et al., 2010; Gong & Piazza, 2013), which can deteriorate the phase noise of the oscillator. Resonators can also be classified based on their vibration modes as either flexural or bulk mode devices. Bulk mode devices typically exhibit high stiffness, and are consequently less prone to thermoelastic damping and consequently achieve large quality factors, even at atmospheric pressure (Xie et al., 2008; Clark et al., 2005; Elsayed et al., 2013b; Lin et al., 2004a; Elsayed et al., 2011; Elsayed et al., 2013a).

In order to implement an oscillator with a MEM resonator, a transimpedance amplifier (TIA) needs to be interfaced with the resonator in a positive feedback loop to sustain a steady-state oscillation by converting the resonator driving current to an output voltage signal (Nabki et al., 2009; Lin et al., 2004a). The sharpness and quality of the output oscillation is usually determined by the quality factor of the resonator and the contributed noise of the TIA. To sustain oscillation, it is necessary for the TIA to have high transimpedance gain due to the resonator insertion loss caused by its motional resistance. Large bandwidth is also required to ensure that the oscillator phase shift at resonance frequency is around 0°, when the MEMS-based oscillator operates in series resonance mode (He et al., 2009). Furthermore, low input and output impedances are required to minimize the resonator Q-factor loading. Several transimpedance topologies have been reported in the literature for MEMS-based oscillator purposes (Salvia et al., 2009; Zuo et al., 2010; Nabki & El-Gamal, 2008; Baghelani et al., 2013; Li et al., 2015; Lavasani et al., 2015; Li et al., 2012; Lavasani et al., 2011; Seth et al., 2012; Lin et al., 2004b; Sundaresan et al., 2006; Chen et al., 2013; Li et al., 2015; Huang et al., 2008). While most designs used in (Nabki & El-Gamal, 2008; Baghelani et al., 2013; Lavasani et al., 2015; Li et al., 2012) are based on RGC topologies, an inverting amplifier topology was proposed in (Zuo et al., 2010; Lavasani et al., 2015). On the other hand, designs proposed in (Seth et al., 2012; Sundaresan et al., 2006; Huang

et al., 2008) use an automatic gain control circuit to regulate the oscillation amplitude and reduce the resonator mechanical non-linearity effect. A current preamplifier was also introduced in (Lavasani et al., 2011). Furthermore, most TIAs use a single-ended architecture (Li et al., 2015; Lavasani et al., 2015; Li et al., 2012) and gain-bandwidth (GBW) product enhancement techniques (Lavasani et al., 2011) so that TIA performance in terms of input-referred noise and power consumption will be improved. However, singled-ended TIAs demonstrate inferior noise performance to that of fully differential TIAs. Differential topologies can benefit of common-mode noise rejection and even harmonics rejection, and therefore, are more desired in applications requiring low noise operation (Carusone et al., 2011). However, power consumption of fully differential transimpedance amplifier designs in (Seth et al., 2012; Chen et al., 2013) are higher than single-ended TIAs in (Sundaresan et al., 2006; Li et al., 2015; Huang et al., 2008).

0.1 Thesis contributions

This dissertation focused on the realization of CMOS transimpedance amplifier capable to interface with series-resonant MEMS oscillator applications. As the result of this research effort, two micromechanical reference oscillators based on both piezoelectric and capacitive MEMS resonators are demonstrated. The MEMS resonators presented here are developed by Dr. Mohannad Y. Elsayed in previous works (Elsayed et al., 2016; Elsayed & Nabki, 2017). The major contributions of the work presented in this thesis outlined as follows:

0.1.1 Non-linear modeling of clamped-clamped MEMS resonator

A non-linear analog hardware description language (AHDL) model for a clamped-clamped beam resonator is presented. The model captures the electrical and mechanical non-linear effects, and accounts for the spring softening and Duffing behavior present

in resonators at high drive levels. A transimpedance amplifier is designed in 0.13 μm CMOS to implement and simulate a MEMS-based oscillator incorporating the Verilog-A model.

0.1.2 Design of a transimpedance amplifiers for MEMS-based oscillators

Detailed study of two transimpedance amplifiers is presented. This study covered both frequency and noise analyses in detail. The first transimpedance amplifier is suitable for oscillators based on capacitive resonators since their motional resistance is high, thus a sustaining oscillation can be achieved with higher gain. The second transimpedance amplifier is suitable for oscillators based on piezoelectric resonators. Since the motional resistance of piezoelectric resonators is higher than the capacitive resonators, despite lower quality factor efficiency, a sustaining oscillation can be achieved with lower gain. Both TIAs are fully differential and fabricated in a Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm process with high gain-bandwidth product where tunable gain and bandwidth separately feature is introduced. Finally, the measured performances of MEMS-based oscillators are demonstrated and compared with state-of-the-art oscillators.

0.2 Thesis outline

This thesis is organized in the following manner. Chapter 1 provides an overview of MEMS-based oscillators. In this chapter a Verilog-A model of clamped-clamped beam resonator is presented. The phase noise performance dependence on the resonator nonlinear effects and its DC polarization voltage are illustrated through simulations.

Chapter 2 and Chapter 3 describe the design and optimization of the fully differential high-performance oscillators based on piezoelectric and capacitive resonators, respectively. The topics covered in these chapters include the performances of TIAs in terms of frequency and noise responses. The open-loop and closed-loop performances of both

capacitive and piezoelectric micromechanical oscillators are also covered. Finally, design trade-offs and their measured performance are provided including a comparison to the state-of-the-art.

CHAPTER I

MEMS RESONATOR MODELING

1.1 Introduction

Reference oscillators are of great interest because of their ubiquitous use in timing applications and in modern wireless communication devices. MEMS based oscillators offer advantages over that of traditional quartz crystal-based oscillators which perform as the resonant filter in such oscillators. However, MEMS resonators exhibit non-linear behavior and lower power handling capability in comparison to quartz crystals and are not as easy to model in circuit simulators in order to account for these particularities (van Beek & Puers, 2012).

MEMS resonator can be modeled in different ways. Lumped electrically equivalent linear models (i.e., RLC resonators) can be used, but are solely linear and do not directly account for the variation of the MEMS resonator with bias voltage. On the other hand, to include the non-linear effects present in MEMS resonators, several methods can be employed. Due of its electromechanical nature, the MEMS resonator exhibits different electrical and mechanical non-linearities (Agrawal et al., 2013), and these must be included in models that allow for the resonator to be faithfully represented in circuit simulations. Traditionally, finite element methods are used to model MEMS devices. Unfortunately, such analyses lead to models that cannot be readily used in circuit simulators, that do not model the resonator non-linearity faithfully, or that are cumbersome

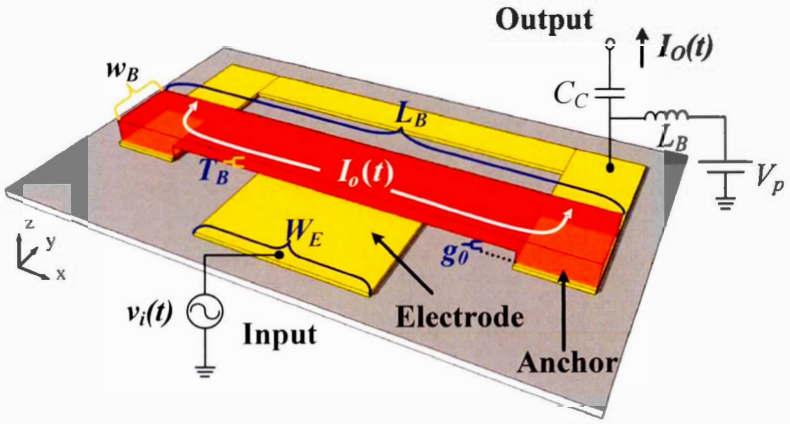


Figure 1.1: Clamped-clamped beam resonator diagram (Nabki et al., 2009).

to modify when the resonator biasing is changed. The solution to this problem is to perform simulations in a circuit simulator by using an analog hardware description language (AHDL) to model the MEMS resonator in a non-linear fashion (Konishi et al., 2013). This allows for a single simulation platform environment that can faithfully represent the resonator.

Accordingly, in this work, a resonator model is implemented using an AHDL: Verilog-A. A transimpedance amplifier (TIA) is also designed in order to implement a MEMS oscillator with the resonator. First, the resonator model is presented, and is then integrated with the TIA to show the impact of the non-linear model on the MEMS oscillator performance.

1.2 Theoretical background

The resonator is composed of a micro-beam which is clamped at both ends and suspended above an electrostatic actuation electrode, as shown in Figure 1.1. While in operation, a DC polarisation voltage, V_P, is applied across the device in addition to the signal.

1.2.1 MEMS resonator analytical models

A lumped electrical model can be used as a small-signal model for the resonator. While this model is a good starting approximation of several parameters such as motional resistance behavior, resonance frequency and quality factor, it ignores electrostatic and mechanical non-linear effects inherent to the C-C resonator (Van Caekenberghe, 2012). The expression of the electrostatic force for a C-C beam resonator is given by

$$F_e(x(t)) = \frac{1}{2}\frac{\partial}{\partial x}C(x(t))V(t)^2, \tag{1.1}$$

where $V(t)$ is the voltage applied across the C-C beam, composed of a bias and signal voltage, and $C(x(t))$ is given by (1.2), where the fringing capacitance has been neglected:

$$C\left(x(t)\right) = \frac{\epsilon_0 A}{g_0 + x(t)}. \tag{1.2}$$

In (1.2), ϵ_0 is the free space permittivity, A is the electrode area, g_0 is the actuation electrode gap and $x(t)$ is the resonator displacement, later labeled as x for simplicity.

The spring force is traditionally proportional to the displacement through the linear spring constant k based on Hooke's law (Senturia, 2000). However, with a C-C beam, the spring force becomes non-linear with sufficiently large beam displacement and its expression is given by (Rebeiz, 2004):

$$F_s(x) = k_1\, x + k_3\, x^3, \tag{1.3}$$

where k_1 is the linear spring constant in the spring force given by (1.4) and k_3 is the cubic spring constant given by (1.5):

$$k_1 = m\,\omega_0^2, \text{ and} \tag{1.4}$$

$$k_3 = \frac{\pi^4 E\, W_r\, t_r}{8 L_r^3}, \tag{1.5}$$

where E is Young's modulus of structural material and L_r, W_r and t_r are the C-C beam resonator dimensions, specifically its length, width and thickness.

Constant κ is the amplitude-frequency (A-f) coefficient and is an important parameter to determine if the resonator will exhibit spring softening or spring hardening behavior (Lee et al., 2011). It is defined as

$$\kappa = \frac{3}{8}\frac{k_{e3}}{k_{e1}}\omega_0, \tag{1.6}$$

where k_{e1} and k_{e3} are the effective fundamental and cubic spring constants, respectively, and are defined as (Mestrom et al., 2009):

$$k_{e1} = k_1 - 2C_0\frac{V_P^2}{g_0^2}, \text{ and} \tag{1.7}$$

$$k_{e3} = k_3 - 4C_0\frac{V_P^2}{g_0^4}, \tag{1.8}$$

where C_0 is the overlap capacitance. These take into account the effects of the electrostatic actuation of the resonator on the mechanical spring constants.

The equation of motion (EOM) of the resonator can be mapped to a single degree-of-freedom (1-DOF) mass-spring-damper system given by (Mestrom et al., 2008):

$$m\,a + d\,v + k_1\,x + k_3\,x^3 = F_e(x), \tag{1.9}$$

where a is the acceleration, d is the damping factor and v is the velocity of the mass. A 1-DOF model simplifies the modeling of the resonator, but it must take the resonant mode-shape into account to accurately model the resonator. For this purpose, the effective mass and gap capacitance can be rewritten to include the electrostatic force non-linear effects. These are given by (Lin et al., 2004a; Nabki, 2010)

$$m = \rho W_r t_r \int_0^{L_r} X_{mode}^2(l)\,\mathrm{d}l, \text{ and} \tag{1.10}$$

$$C(t) = \epsilon_0 W_r \int_{L_e} \frac{\mathrm{d}l}{g_0 + \tau(t)X_{mode}(l)}, \tag{1.11}$$

where ρ is the density of the structural material, L_e is the electrode length, X_{mode} is the beam mode shape that depends on position l on the beam and $\tau(t)$ is the time function

that describes the position of the beam during vibration and can substitute x in (1.9). Note that the model supports different mode shapes, but only the first C-C mode is considered here, as it can be readily isolated in single resonator systems.

In response to the resonant motion, an output current is generated and is given by

$$i_{out}(t) = \frac{\mathrm{d}}{\mathrm{d}t} C(t) V(t) \tag{1.12}$$

1.3 System description

1.3.1 AHDL model

A Verilog-A code was written to model the C-C beam resonator based on (1.1), (1.3)-(1.5) and (1.9)-(1.12). The functional diagram of the code is shown in Figure 1.2. Initially, the integrator outputs is calculated with initial position, x_0, and the output current, i_{out}, can be calculated with the given input voltage, v_{in}. Afterwards, the beam position is calculated within the mechanical and electrical modules where the equivalent forces will take part in the EOM solver.

The AHDL in SpectreRF supports only time-domain integration but not the integration of functions having variables other than time. Accordingly, the integration described in (1.10) and (1.11) is replaced by numerical integration. Several methods exist in numerical analysis to represent integration (Burden & Faires, 2011). The *Legendre-Gauss Quadratic* method was selected in this work. Its equivalent expression is given by

$$\int_a^b f(x)\,\mathrm{d}x \approx \frac{b-a}{2} \sum_{i=1}^{N} w_i\, f\left(\frac{b-a}{2} x_i + \frac{a+b}{2}\right), \tag{1.13}$$

where $f(x)$ is the function to be integrated, a and b are the integral limits, N is the number of points, w_i and x_i are weight and position point, respectively, for the numerical integration. Coefficients w_i et x_i are calculated within the Verilog-A code.

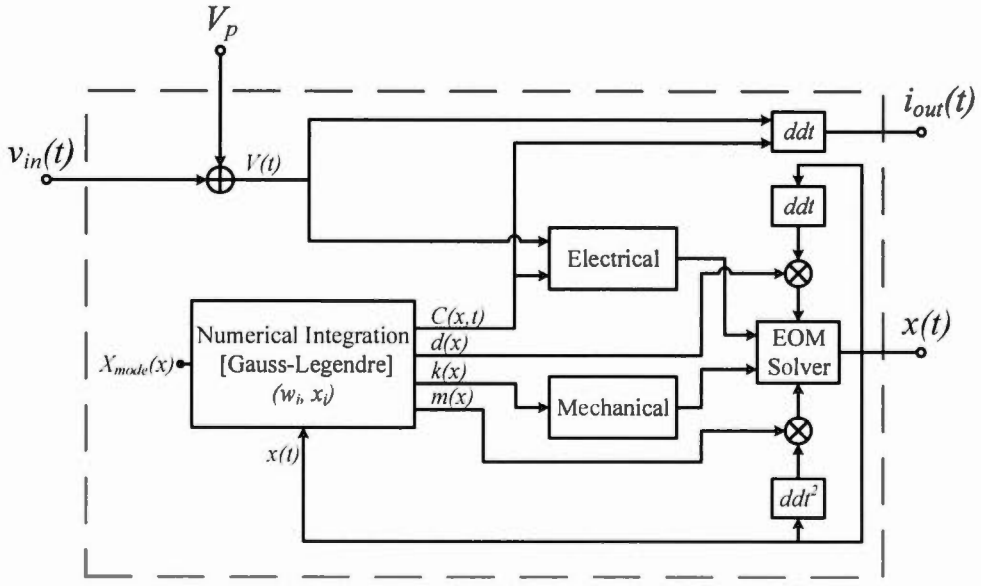


Figure 1.2: Verilog-A functional diagram.

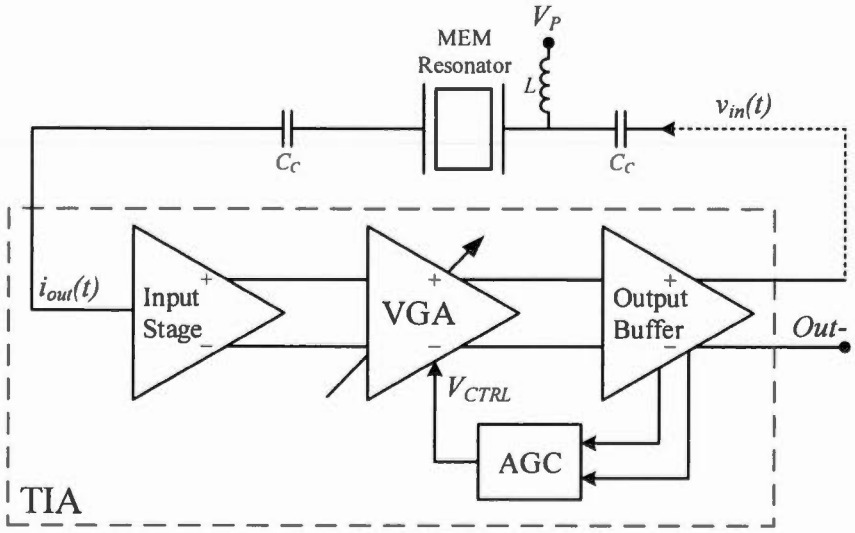


Figure 1.3: MEMS-based oscillator with expanded TIA block diagram.

1.3.2 MEMS oscillator system overview

An oscillator consists of a MEMS resonator and a TIA, as shown in Figure 1.3. The

TIA was designed in 0.13μm CMOS. To minimize the quality factor loading (Lin et al., 2004a), a regulated cascode was used as input stage in order to obtain smaller input resistance, R_{in}. An output buffer was also designed in order to obtain smaller output resistance, R_{out}. A variable gain amplifier (VGA) alows for the gain of the TIA to be tuned with voltage V_{ctrl}. The gain of the TIA is controlled by an automatic gain control (AGC) loop (Nabki & El-Gamal, 2008). Note that the polarisation voltage of the MEMS resonator, V_P, is applied with a bias tee. To sustain oscillation in closed-loop, the following Barkhausen criteria are required (van Beek & Puers, 2012; Lin et al., 2004a):

$$\phi_{TIA} + \phi_{MEMS} = 0°, \text{and} \tag{1.14}$$

$$Z_T \geq R_m + R_{in} + R_{out}, \tag{1.15}$$

where ϕ_{TIA} and ϕ_{MEMS} correspond to the phase shifts of the TIA and resonator, respectively, and Z_T is the transimpedance gain of TIA. In this case, both resonator and TIA must have 0° phase shift.

1.4 Simulation results

Table 1.1 summarizes the overall oscillator circuit design parameters and simulated TIA performance metrics.

1.4.1 MEMS resonator open-loop behavior

Before undertaking circuit simulation, the optimal number of points, N, to be included into the numerical integration block of the Verilog-A model was determined. The number of points used in the integration block is equivalent to dividing the resonator beam into equal sections with relative motions characterized by the resonator mode-shape and time function. As shown in Figure 1.4, the simulation time is a linear function of N. The optimal number of sections is attained at N_{opt} = 7 when the phase shift converges to 1.58°. In this work, simulations were performed with 60 beam sections in order to

Table 1.1: Oscillator design parameters and TIA performance metrics

	Parameter	**Value**	**Unit**
Lumped model	Motional resistance, R_m	1.55	kΩ
	Motional inductor, L_m	91.56	mH
	Motional capacitance, C_m	4.26	fF
	Feedthrough capacitance, C_0	71.24	fF
AHDL model	Beam width, W_r	10	μm
	Beam length, L_r	45	μm
	Beam thickness, t_r	2	μm
	Gap, g_0	100	nm
	Electrode length, L_e	23	μm
	Center frequency, f_0	8.061	MHz
	Young's modulus, E	150	GPa
	Mass density, ρ	2.330	kg/m^3
	Quality factor, Q	3000	-
	Polarisation voltage, V_P	6	V
	A-f coefficient, κ	< 0	rad/s
TIA	Input impedance, R_{in}	89	Ω
	Output impedance, R_{out}	86	Ω
	Bandwidth	26	MHz
	Gain, Z_T	103	dBΩ
	Power supply, V_{DD}	1.2	V
	Power consumption, P_{DC}	2.16	mW

operate the model at a high complexity level to demonstrate its computational stability with a large number of beam sections. To illustrate the non-linear effects included by the resonator model, several simulations were run. Figure 1.5 shows the resonator frequency response at different input power levels. The power levels were chosen to represent small, medium and large output oscillations which are given by -50, -35 and -15 dBm, respectively. The results indicate spring softening non-linear behavior, as

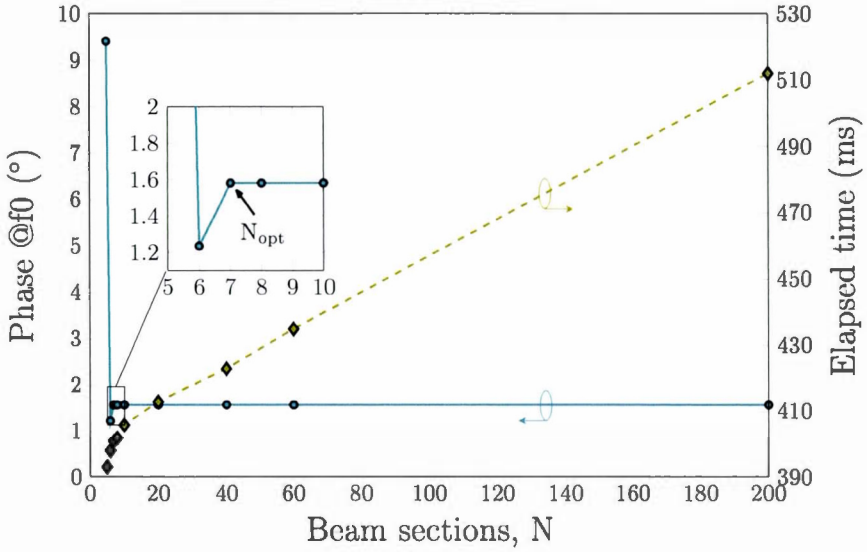


Figure 1.4: Resonator phase shift at resonance frequency (solid line) and simulation elapsed time (dashed line).

typically seen in these type of resonators. As shown in Figure 1.5(a), for smaller amplitude, the resonator has a linear transmission characteristic. With increasing amplitude, the non-linear effects appear with increased insertion loss and Duffing behavior. Figure 1.5(b) shows the amplitude-frequency curve with the same power levels. As can be seen, the non-linearity effect begins to appear at the medium power level, and at -15 dBm, the resonator becomes sufficiently non-linear for its frequency response to be characterized by cyclic fold bifurcations.

Also, the resonator DC bias voltage, V_P, has an effect on the frequency response since it is included in the resonance frequency expression (Lin et al., 2004a). As shown in Figure 1.6, increasing the DC bias voltage reduces the resonance frequency. Using an RLC resonator, it is hard to obtain such curves before having to recalculate its parameters for each bias voltage, and the non-linear effect previously shown cannot be modeled effectively.

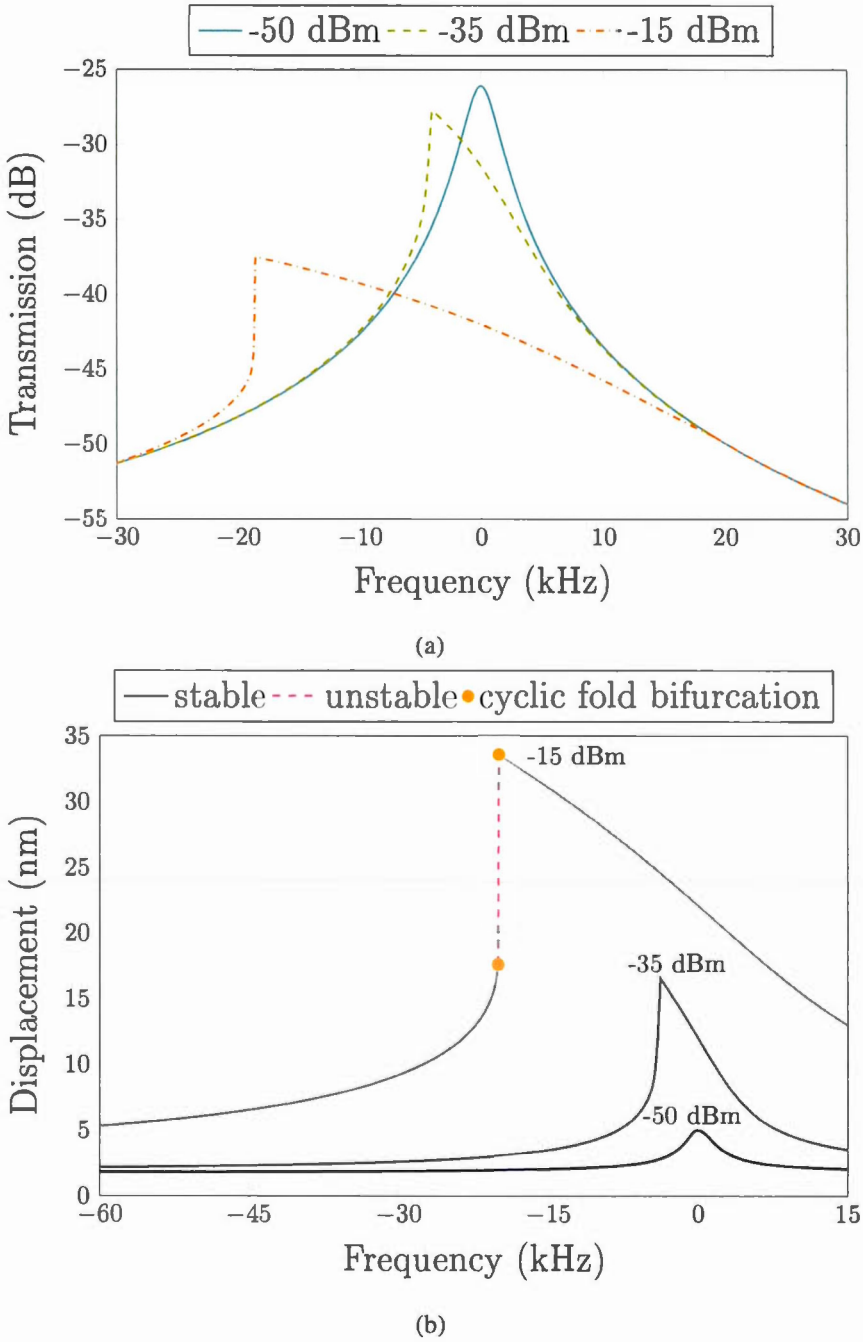


Figure 1.5: (a) Transmission characteristic and (b) displacement amplitude-frequency curve for various output amplitude levels.

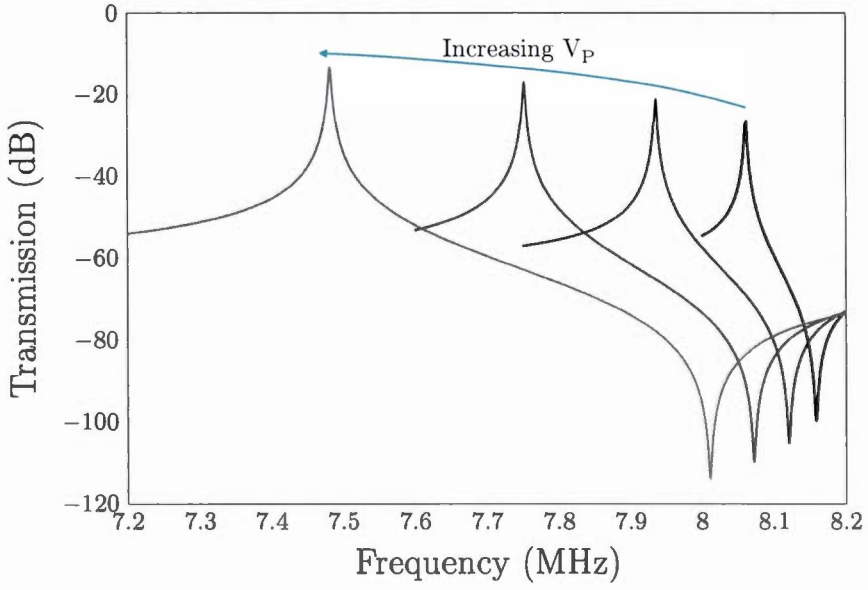


Figure 1.6: Transmission characteristic for various DC bias voltage levels starting from 6 V to 12 V.

1.4.2 Oscillator phase noise

The overall circuit was simulated using the closed-loop configuration, as shown in Figure 1.3. The start-up response is shown in Figure 1.7 using 6 V and 10 V DC bias voltages. The response with 10 V biasing is faster than with 6 V due to the reduced insertion loss of the resonator at a higher bias voltage. The oscillator phase noise was characterised in three simulations with different output oscillation levels, and the results are listed in Table 1.2. The resulting RMS phase jitter is also listed as it is an important metric in oscillators used in timing applications. Due to non-linear effects leading to noise folding, the close-in phase noise and jitter performance is worsened at the higher oscillation level suggesting an optimal resonator drive level.

To verify the influence of V_P on the phase noise, a 1 μV 100 kHz harmonic source was added to the bias line. Figure 1.8 shows the phase noise in closed-loop with two

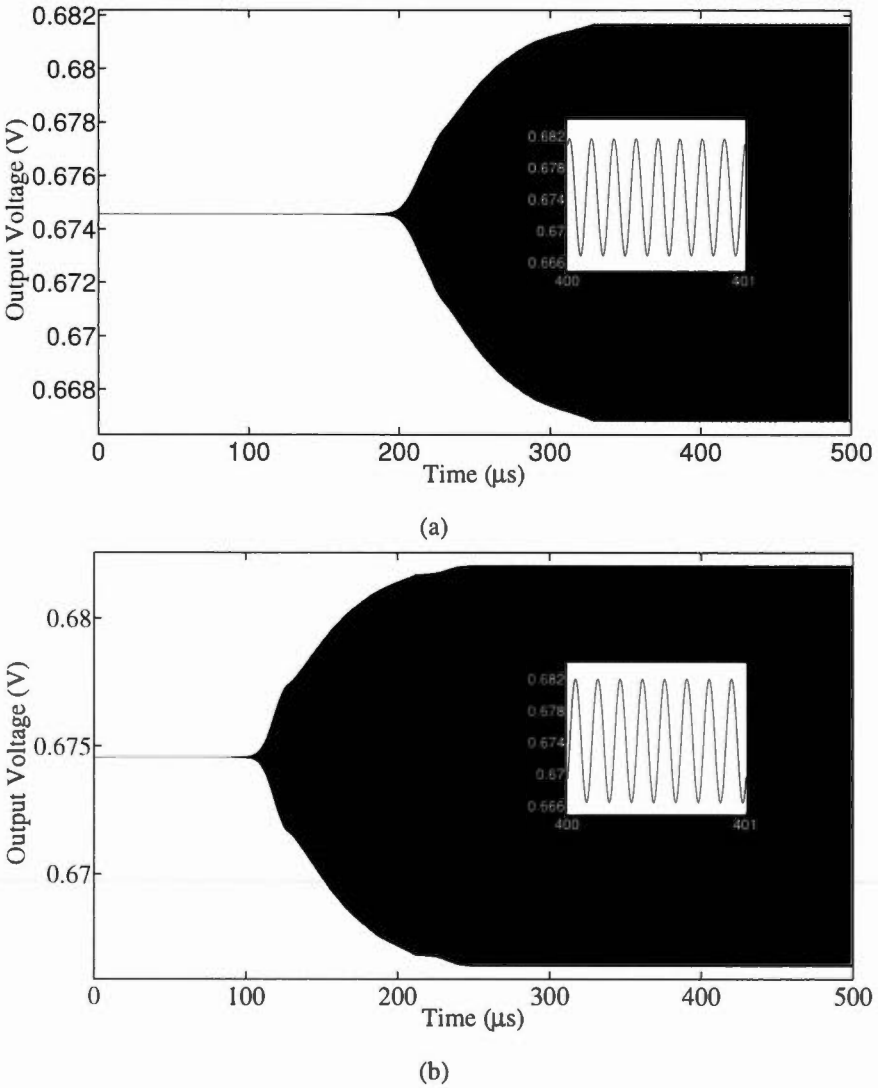


Figure 1.7: Start-up response of MEMS-based oscillator in closed-loop for (a) V_P=6V and (b) V_P=10V.

different V_P values. In this case, two spurs are seen in each curve. The first spur is the effect of the added interference source, while the second is related to the oscillation itself. The detrimental effects of non linearity on se noise can be seen at a bias of 10 V, where the close-in phase noise performance is dominated by resonator non-linearity and not the TIA flicker noise seen with a 6 V bias. All of the above-mentioned effects

Table 1.2: Oscillator noise performance for V_P = 10 V.

Oscillation Level (dBm)	-15	-35	-50
Phase Noise @ 100 Hz (dBc/Hz)	-65.69	-73.02	-34.56
Phase Noise @ 100 kHz (dBc/Hz)	-119.9	-104.2	-83.82
RMS Phase Jitter (ns) (100 Hz to 100 kHz offset)	6.25	1.51	131.17

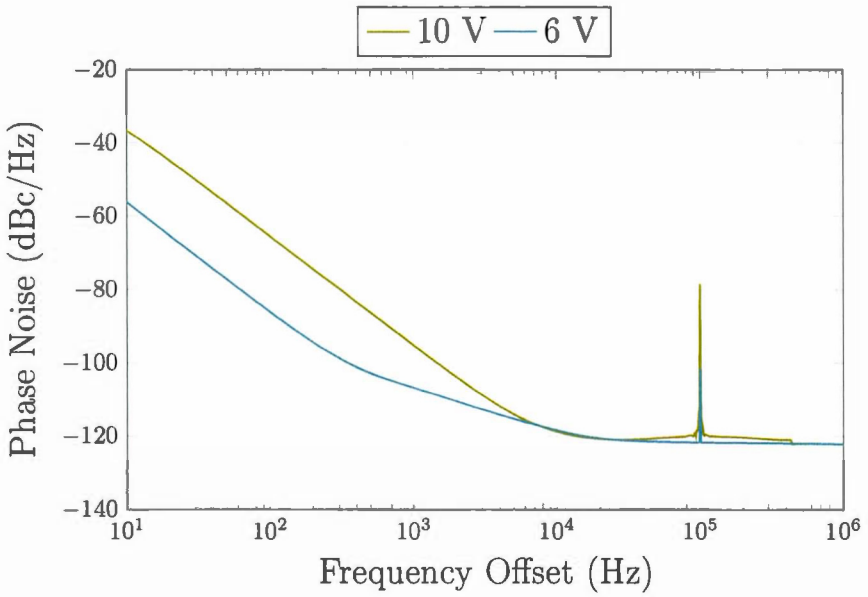


Figure 1.8: Phase noise plot for two different DC polarisation voltages with a harmonic noise source.

would not be modeled by a lumped RLC linear model, outlining the importance of taking into account non-linearities and bias voltage when designing MEMS oscillators.

1.5 Conclusion

A non-linear AHDL model for a C-C beam resonator was presented. The non-linear frequency response and the effects of the bias voltage were described. An oscillator was designed in a 0.13 μm technology to demonstrate the use of the model in a circuit, and closed-loop simulations illustrated the impact the non-linear and biasing effects of

the MEMS resonator on the performance of the MEMS-based oscillator. Ultimately, the model captures several effects such as Duffing behavior or phase noise degradation when overdriving the resonator that cannot be modeled by a linear model.

CHAPTER II

OSCILLATOR BASED ON PIEZOELECTRIC RESONATOR

2.1 Piezoelectric disk resonator overview

The resonator used in this work is presented in (Elsayed et al., 2016). A brief overview is given in this section. The resonator is based on a disk structure that is exciting through piezoelectric actuation. A diagram of the resonator is shown in Figure 2.1. The device is composed of a single-crystalline silicon central disk structure acting as the main resonator structure. This disk is 10 μm thick and has a 200 μm diameter. It is covered by a 0.5 μm layer of aluminum nitride (AlN), the piezoelectric material used for transduction. The disk structure is supported by four suspension beams having a 10 μm width (the minimum allowed by the design rules of the MEMS fabrication technology) with 90° angular spacing, so as to correspond with the nodal points of the bulk wine-glass resonance mode. The support beams are anchored to the substrate at their ends and mechanically connected to the electrical pads. Each of these supports is associated with a pair of pads, one for the signal routed above the piezoelectric layer, and the other for the ground, routed through the underlying silicon structural layer. For this purpose, an aluminum layer above the disk structure is patterned into four distinct quadrants, in order to match the strain distribution and yield differential input/output ports. Each electrode is electrically connected to a distinct signal pad by an aluminum track routed above its respective suspension beam. The conductive structural silicon layer itself acts as the

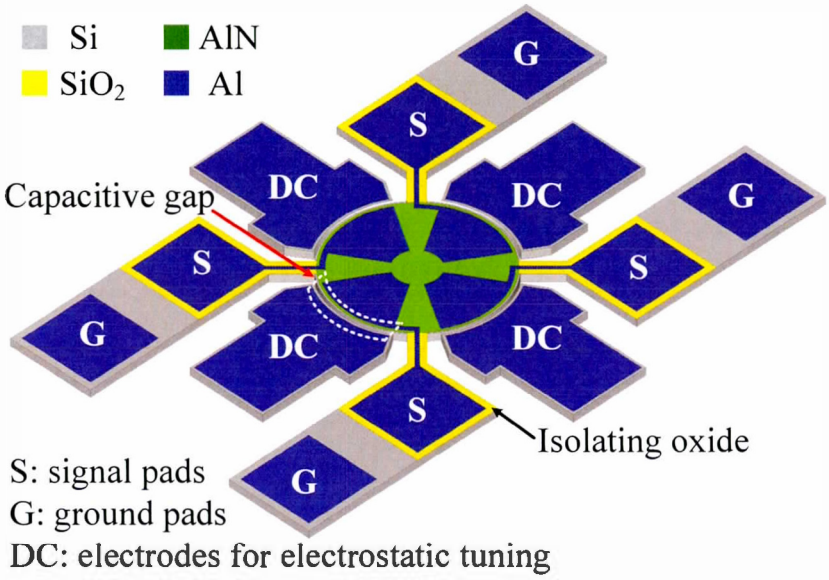


Figure 2.1: Simplified diagram of the disk resonator outlining the pads used for differential piezoelectric driving by the TIA and the pads used for electrostatic tuning (Elsayed et al., 2016).

ground plane of the device, and connects with each ground pad while remaining electrically insulated from the signal track by a layer of silicon dioxide. Aluminum nitride is not present on the supports to avoid any unintended transduction which would alter the resonance mode and possibly lead to undesirable spurious modes of vibration. Capacitive electrodes are placed around the disk structure for optional electrostatic tuning of the resonance frequency, based on the electrostatic spring softening phenomenon.

2.2 Transimpedance amplifier circuit design

The transimpedance amplifier circuit shown in Figure 2.2 is composed of three fully differential stages: *i*) an input stage followed by *ii*) a variable gain amplifier (VGA) and *iii*) an output stage based on a super source follower (SSF). An automatic gain control circuit (AGC) is also included to regulate the oscillation amplitude and reduce the

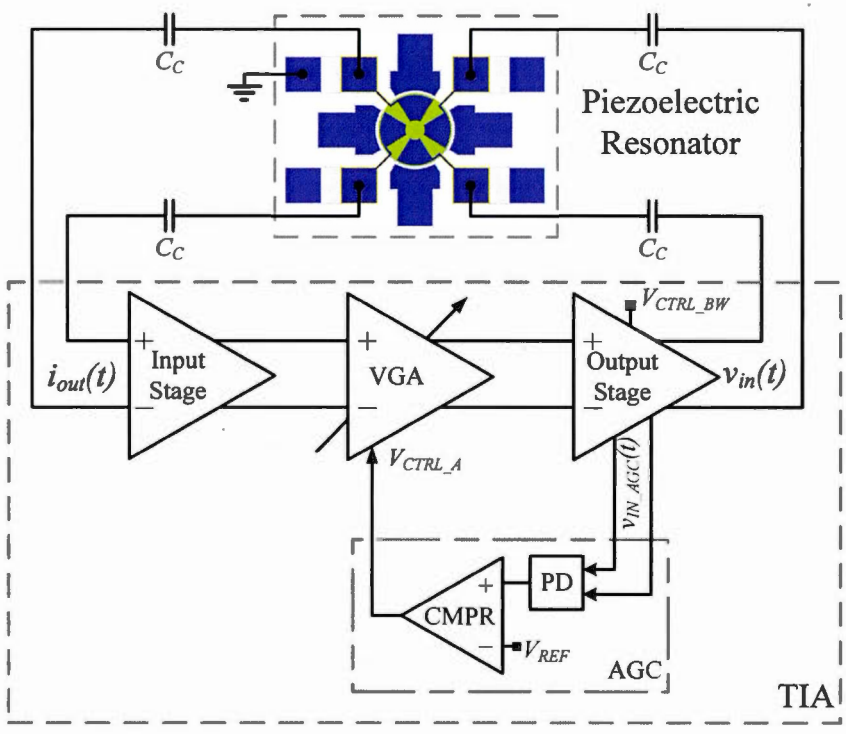
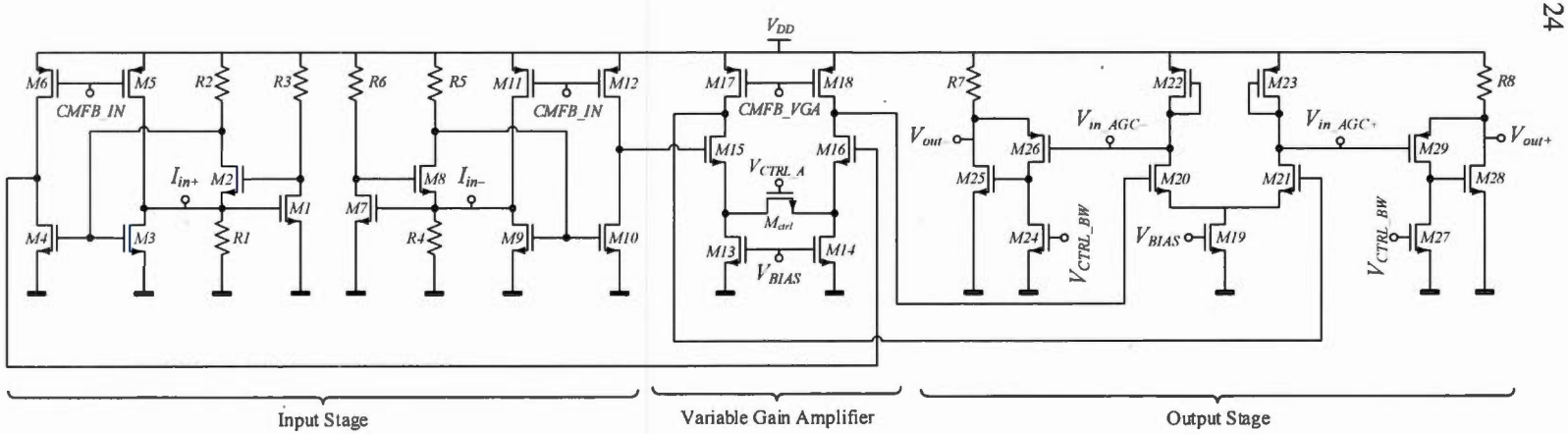


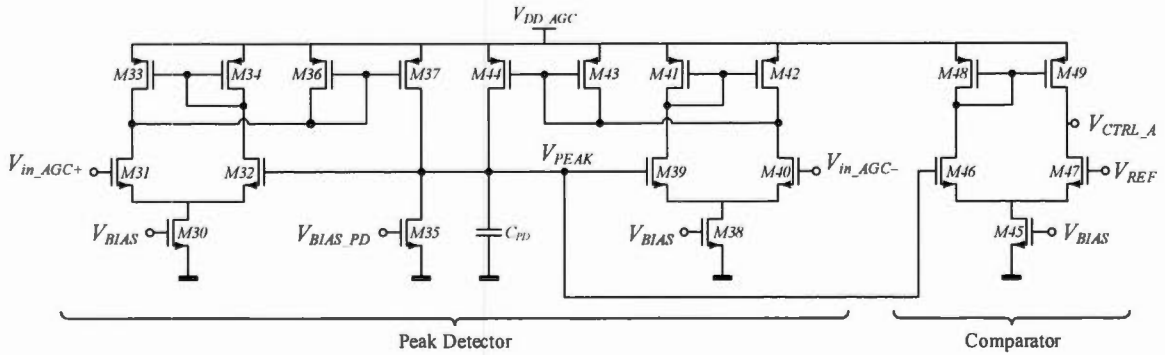
Figure 2.2: MEMS-Based Oscillator functional diagram.

exertion of the resonator's mechanical non-linearity, thereby improving the oscillator frequency stability (Lee & Nguyen, 2003).

The complete schematic of the TIA circuit is shown in Figure 2.3 in which the biasing and common-mode feedback (CMFB) circuits are not shown. The TIA provides low input impedance (R_{in}) and low output impedance (R_{out}) so as to compensate a large parasitic interconnect capacitance (C_P = 4 pF) and push the dominant pole far beyond the oscillation frequency, while reducing the loading on the resonator's quality factor. This translates into a high GBW product requirement (Pettine et al., 2012).



(a)



(b)

Figure 2.3: Circuit schematic of (a) the proposed fully differential TIA design, and (b) the AGC circuit.

2.2.1 Input stage

The input stage should be carefully designed in such a way to satisfy several criteria. Besides the high GBW product criterion, tradeoffs between lower input impedance, power consumption and current noise are also other key performance parameters to be considered when designing the intput stage. Three input stage topologies (Sackinger & Guggenbuhl, 1990; Salvia et al., 2009; Kopa & Apsel, 2008) were selected to be compared with the proposed input stage by means of circuit performance simulations using the SpectreRF simulator in a CMOS 65 nm technology. The first design (Sackinger & Guggenbuhl, 1990) is based on gm-boosted common-gate (CG) topology, known as regulated cascode (RGC) input stage and described in (Nabki & El-Gamal, 2008). The second topology is the common source feedback (CSFB) amplifier presented in (Kopa & Apsel, 2008). The CSFB technique is used to amplify current, which enhances the bandwidth by reducing the size of the load resistance. The third design considered is based on (Salvia et al., 2009), where capacitive feedback is used as a current amplifier. The input-referred noise of this configuration is expected to be very low because of the absence of noise sources directly at the input (Razavi, 2000).

Each topology has been simulated with an additional shunt parasitic capacitance of $C_P = 4$ pF, and to make a representative comparison of performance, the transimpedance gain was adjusted to be equal ($\sim$ 78 dBΩ). A normalized figure-of-merit (FOM$_1$), which is given by

$$FOM_1 = \frac{\text{Gain}[\Omega] \times BW[MHz]}{P_{DC}[\mu W] \times \text{Noise@}f_0[pA/\sqrt{\text{Hz}}] \times R_{in}[\Omega]}. \tag{2.1}$$

FOM_1 is used to evaluate the overall performance of the TIA input stage.

According to Table 2.1, the capacitive feedback topology exhibits the lowest input-referred current noise, while the CSFB topology exhibits excessive noise. The gain of the RGC input stage is limited by the large load resistor due to the large DC volt-

Table 2.1: Simulated input stage performance comparison with target transimpedance gain of 78 dBΩ (shunt parasitic capacitance C_P = 4 pF).

Spec.	RGC	Caps FB	CSFB	Proposed Work
Bandwidth [MHz]	197	96	246	204
Power consumption, P_{DC} [μW]	161	168	190	180
Input Impedance, R_{in} [Ω]	76	4406	74	69
Input-referred noise @f_0 $\left[pA/\sqrt{Hz}\right]$	5.05	0.89	8.86	3.35
Figure-of-merit, FOM_1	25.34	1.16	15.67	38.95

age drop across it (Park & Toumazou, 2000). The large gain and bandwidth of the CSFB topology can be easily set. However, the limitation of this topology comes from the noise performance. The capacitive feedback topology benefits from current pre-amplification, and the transimpedance gain can be high with a smaller load resistor, unlike resistive feedback topologies. The major drawback of the capacitive feedback topology is that its input impedance is very high at the resonant frequency, which will load a resonator's Q-factor.

In order to benefit of lower input impedance while extending transimpedance gain and bandwidth, the proposed input stage is based on a modified versions of the RGC and CSFB topologies by using active feedback, as shown in Figure 2.3(a).

2.2.1.1 Input impedance

According to the small-signal analysis, the single-ended low-frequency input impedance of the proposed circuit is given by (Yuan & Sun, 2002)

$$R_{in} = \frac{1}{R_{in,\,RGC} \times (1 + R_2\, g_{m3})}, \tag{2.2}$$

where $R_{in,RGC}$ is the input impedance of the RGC circuit which is given by

$$R_{in,\,RGC} = \frac{1}{g_{m2}\,(1 + R_3\, g_{m1})}, \tag{2.3}$$

where g_{m1}, g_{m2} and g_{m3} are the transconductance of transistors $M1$, $M2$ and $M3$, respectively. As indicated by (2.2), the input impedance of the input stage is $(1 + R_2\, g_{m3})$ times smaller than an RGC input stage.

2.2.1.2 Transimpedance gain

The expression for the input stage transimpedance gain is given by

$$Z_T(s) \cong \frac{\left(\frac{R_{in,o}\, g_{m4}}{g_{m3}}\right)\left(1 + s\frac{R_3 C_1}{1 + R_3 g_{m1}}\right)}{(1 + sR_{in}C_{in})\,(1 + sR_3C_1)\,(1 + sR_2C_2)\,(1 + sR_{o,in}C_{out})}, \tag{2.4}$$

where C_{in} and C_{out} are the total input and the output capacitances of the input stage, respectively, C_1 is the equivalent capacitance between the drain of $M1$ and gate of $M2$, C_2 is the equivalent capacitance between the drain of $M2$ and gate of $M3/M4$, and $R_{o,in}$ is the output impedance of the input stage which is given by $R_{o,in} = r_{o4} \parallel r_{o6}$, where r_{o4} and r_{o6} are the output resistances of transistors $M4$ and $M6$, respectively. The DC transimpedance gain is given by

$$Z_T(0) \cong \frac{R_{out}\, g_{m4}}{g_{m3}}, \tag{2.5}$$

where g_{m4} is the transconductance of transistor $M4$.

2.2.1.3 Bandwidth

It can be seen from (2.4) that the 3-dB bandwidth of the input stage is limited by the dominant pole appearing at the drain of transistor $M2$ and is given by

$$f_{-3dB} \cong \frac{1}{2\pi R_2 \times \left[C_{gd2}\left(1 + \frac{R_1}{R_2}\right) + C_{gs3} + C_{gd3} + C_{gd4}\, g_{m3}\, r_{o4}\right]}, \tag{2.6}$$

where $C_{gd,i=\{2,3,4\}}$ are the gate-drain capacitances of transistors $M2$, $M3$ and $M4$, respectively, and C_{gs3} is the gate-source capacitance of transistor $M3$.

The local feedback of the input stage creates a zero at a frequency given by

$$f_z = \frac{1 + R_3\, g_{m1}}{2\pi R_3\, C_1} \cong \frac{g_{m1}}{2\pi C_1}. \tag{2.7}$$

To keep the zero far away from the dominant pole (Park & Yoo, 2004), the transconductance g_{m1} of transistor $M1$ should be increased, i.e. increasing its width. However, increasing the width of $M1$ will significantly increase capacitance C_1, specifically the equivalent capacitance of the drain of $M1$, and will reduce the zero frequency. Instead, capacitance C_1 can be reduced by reducing the width of transistor $M2$ to decrease the equivalent capacitance at its gate. This will affect the input impedance of the the RGC stage in (2.3) since the transconductance g_{m2} of transistor $M2$ will be decreased. However, this will not critically affect the input impedance of the RGC stage or the input stage since g_{m2} is proportional to $\sqrt{(W/L)_2}$, while its gate capacitance is linearly proportional to $(WL)_2$.

On the other hand, decreasing the input impedance amounts to increasing $(1 + R_2\, g_{m3})$ or $(1 + R_3\, g_{m1})$. The former will affect the DC TIA gain and the input stage bandwidth. Therefore, increasing R_3 is selected as the method for input impedance reduction.

2.2.1.4 Noise analysis

The input-referred current noise is an important performance parameter to be considered when designing the proposed TIA. It can be used to provide a representative comparison between different circuit topologies (see Table 2.1). Since the noise is mostly contributed by the input stage, then the noise of the other stages can be neglected to simplify the analysis. Therefore, a noise analysis was carried-out based on the analysis method proposed in (Park & Yoo, 2004) where shot noise and flicker noise are ignored. Assuming that all noise sources are uncorrelated, the input-referred current noise for

the input stage is calculated and its expression is given by

$$\overline{i_{n,in}^2} = 4kT\left(\frac{1}{R_1} + \gamma\, g_{d0,3}\right) + \frac{4kT\gamma\omega^2 C_{out}^2}{g_{m4}^2}(g_{d0,4} + g_{d0,6}) + \frac{\omega^2(C_1+C_2)^2}{g_{m2}^2}\left(\gamma\, g_{d0,2} + \frac{1}{R_2}\right) + \frac{4kT\left(\frac{1}{R_1^2} + \omega^2 C_{in}^2\right)}{\left(g_{m1} + \frac{1}{R_3}\right)^2}\left(\gamma\, g_{d0,1} + \frac{1}{R_3}\right), \tag{2.8}$$

where γ is the noise coefficient (Shaeffer & Lee, 1997; Ogawa, 1981), k is Boltzmann's constant, T the absolute temperature and $g_{d0,i=\{1-6\}}$ are the zero-bias drain conductances of transistors $M1$-$M6$, respectively.

From (2.8), the noise can be analysed as follows: the thermal noise and the channel thermal noise contributions from R_1 and $M3$, respectively, are directly applied to the equivalent input noise. As the frequency increases, the noise is dominated by terms containing ω^2. Therefore, to achieve a low noise, resistor R_1 need to be increased and it is preferable to keep the size of transistor $M3$ as small as possible to maintain lower input-referred noise as well as higher transimpedance gain and bandwidth performance. However, reducing the size of $M3$ can increase the input impedance of the TIA, as mentioned earlier, and increasing R_3 can compensate the effect of reducing the size of $M3$, thereby achieving an overall compromise of performance.

2.2.2 Variable gain amplifier

The variable gain amplifier shown in Figure 2.3(a) is based on a differential pair amplifier in which transistors $M15$ and $M16$ form the input pair and $M17$ and $M18$ act as active loads to provide high gain. The source degeneration transistor M_{ctrl} is used in the triode region in order to linearly tune the gain of the VGA over a large range through control voltage V_{CTRL_A}. Assuming that the output resistance of transistors

$M14$ and $M16$ are sufficiently large, the gain of VGA can be expressed as

$$G_{VGA} \cong -g_{ds,ctrl}\, r_{o18} \frac{g_{m15}}{g_{m15} + g_{ds,ctrl}}, \tag{2.9}$$

where r_{o18}, g_{m15}, and $g_{ds,ctrl}$ are the output resistance of transistor $M18$, transconductance of transistor $M15$, and the conductance of the source degeneration transistor M_{ctrl}, respectively. Evidently, if r_{o14} and r_{o16} are too large and $g_{m15} \gg g_{ds,ctrl}$, the gain VGA can rewritten as:

$$G_{VGA} \cong -g_{ds,ctrl}\, r_{o18} \cong -k_{n,ctrl}\, (V_{GS,ctrl} - V_{th,ctrl})\, r_{o18}, \tag{2.10}$$

where $k_{n,ctrl}$, $V_{GS,ctrl}$, and $V_{th,ctrl}$ are the transconductance parameter, gate-source voltage, and threshold voltage of transistor M_{ctrl}, respectively. Consequently, source degeneration transistor M_{ctrl} can linearly control the VGA gain through control voltage V_{CTRL_A}.

2.2.3 Super source follower

The output stage shown in 2.3(a) is based on the SSF topology (Gray et al., 2009). It is based on a differential pair amplifier in which transistors $M20$ and $M21$ form the input pair and are loaded by the diode connected transistors $M22$ and $M23$. The outputs of the differential pair are connected to the AGC circuit for the gain control loop. The SSF is formed by transistors $M24$-$M29$ and resistors $R7$ and $R8$ to drive the fully differential resonator and it is characterized by a small output impedance in order to avoid loading the resonator's Q-factor. The gates of transistors $M24$ and $M27$ are controlled by control voltage V_{CTRL_BW} so that TIA bandwidth can be adjusted to yield the optimal phase loop characteristic.

The gain of the SSF is given by

$$G_{SSF} \cong \frac{g_{m26}\, r_{o26}}{1 + g_{m26}\, r_{o26} + \dfrac{1}{(R_7 \parallel r_{o25})\, g_{m25}}}, \tag{2.11}$$

where g_{m25} and g_{m26}, r_{o25} and r_{o26} the transconductances and output resistances of transistors $M25$ and $M26$, respectively. As can be seen in (2.11), if $g_{m26}\, r_{o26} \gg 1$ and $(R_7 \parallel r_{o25})$ is sufficiently large, the gain of SSF will be close to 1 V/V.

The output impedance of the supper source follower is given by

$$R_{out} = \left\{ (R_7 \parallel r_{o25}) \parallel \frac{r_{o24}}{(1 + g_{m26}\, r_{o26})\,(1 + g_{m25}\, r_{o24})} \right\} \cong \frac{1}{g_{m26}\, r_{o26}\, g_{m25}}, \qquad (2.12)$$

where r_{o24} is the output resistance of transistor $M24$.

The output resistance of SSF is reduced by a factor of $(r_{o26} \times g_{m25})$ in comparison to the conventional source follower, whose output resistance is $\sim 1/g_m$. This enhancement of the output resistance is due to the negative feedback through transistor $M25$.

2.2.4 Automatic gain control circuit

The schematic of the automatic gain control circuit is shown in Figure 2.3(b). The first stage consists of a differential positive peak detector (Wenbo et al., 2013) that monitors the output nodes of the differential pair composed of $M20$-$M21$. The peak detector is based on a differential amplifier ($M31$-$M34$) and a current mirror ($M36$ and $M37$). Transistor $M35$ is used a small current sink to discharge capacitor C_{PD}. The peak of the signal is then compared to an amplitude reference (V_{REF}), and the resulting difference is integrated to control the TIA's gain through (V_{CTRL_A}) connected to M_{ctrl}.

2.3 Experimental results

Two test configuration setups, shown in Figure 2.4, were used to characterize the MEMS oscillator: *i*) the open-loop configuration (solid lines) and *ii*) the closed-loop (dashed lines). A Keysight E5061B vector network analyzer (VNA) was used to measure the two-port S-parameters of the resonator and TIA and as well as the oscillator in open-loop in order to obtain the frequency response. The output spectrum and phase noise of the oscillator were measured with a Keysight N9030A spectrum analyzer.

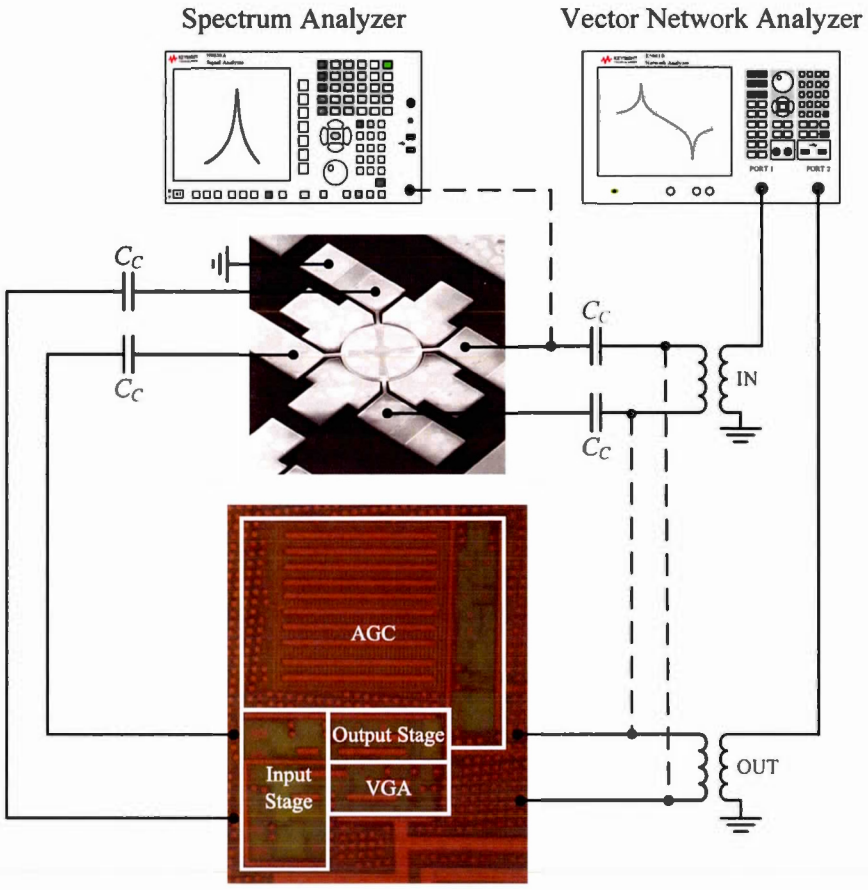


Figure 2.4: Test Setup of the MEMS-based oscillator in open-loop (solid line) and closed-loop (dashed line) with micrographs of the TIA and resonator dies.

2.3.1 Resonator characterization

The frequency response of the resonator was measured in differential configuration with the VNA in air as well as under a vacuum level of 100 mTorr. Different input power levels starting from -20 dBm up to 10 dBm were applied to the resonator. Figure 2.5 shows the transmission characteristic curves normalized to the center frequency of 14.42 MHz with a Q-factor of 4900 under vacuum and 1950 in air. The maximum insertion loss in air and under vacuum is of -29 dB and -22 dB, which corresponds to a motional resistance of 1.2 kΩ and 0.9 kΩ, respectively. Thus, the results indicate

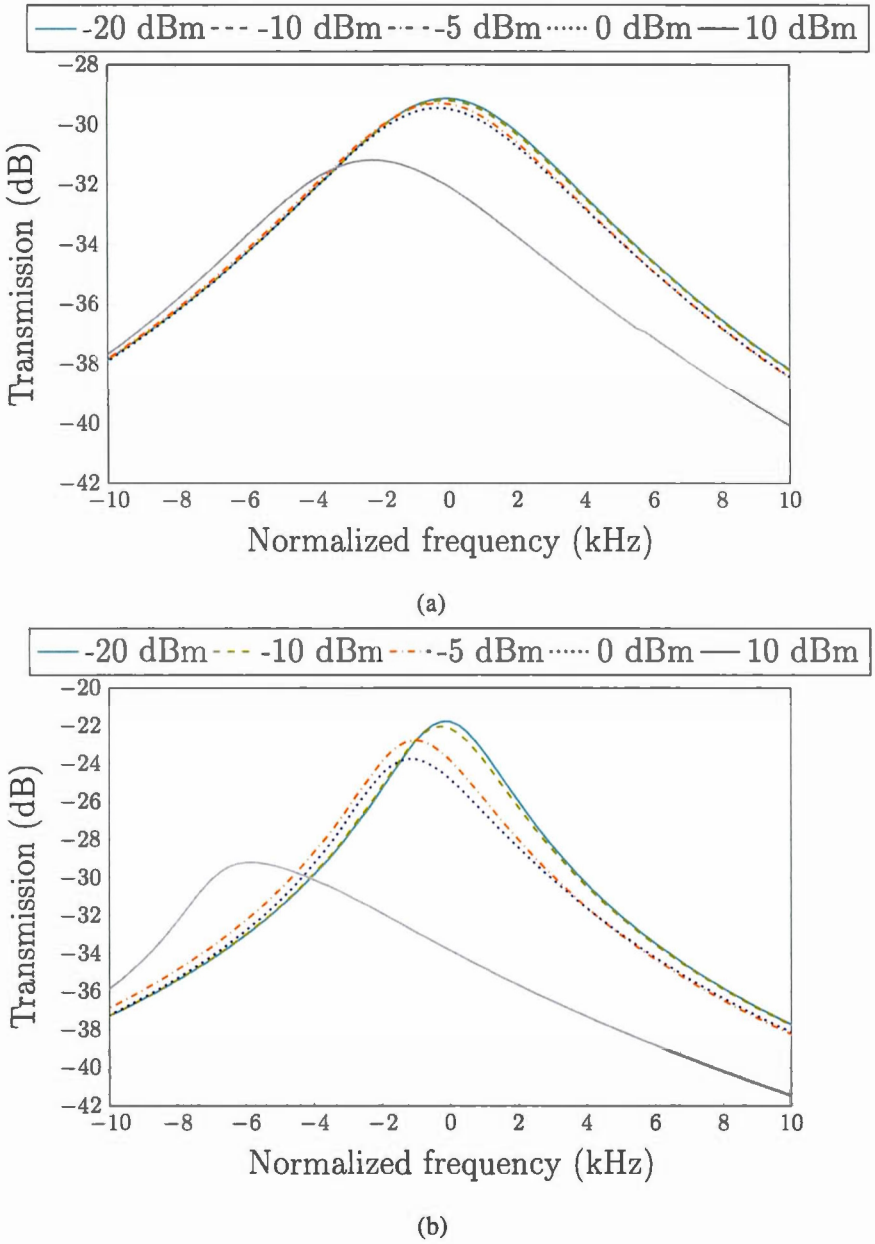


Figure 2.5: Normalized transmission characteristic curve for various input amplitude levels (a) in air, and (b) under vacuum.

spring-softening non-linear behavior stemming from the negative amplitude–frequency (A–f) coefficient (κ) associated with this resonator (Bouchami & Nabki, 2014). The

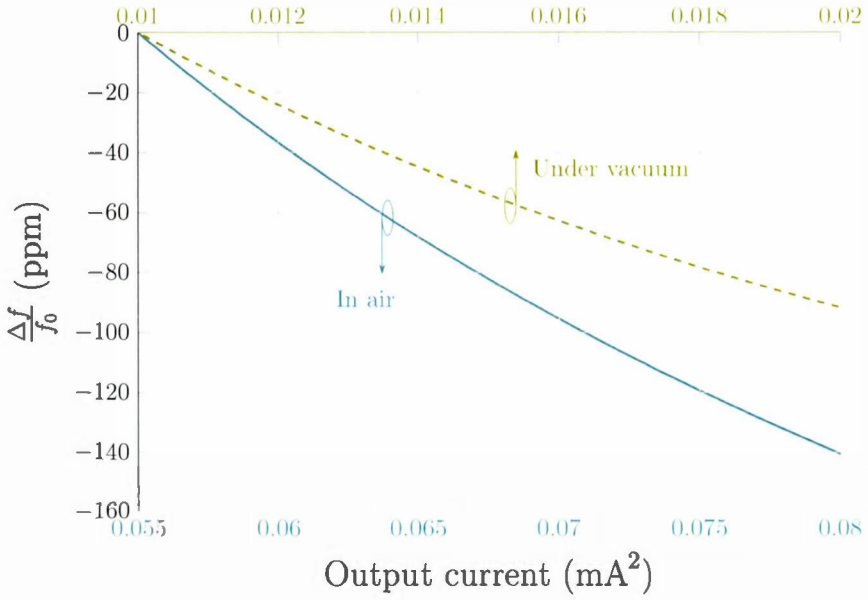


Figure 2.6: Relative resonant frequency shift of the resonator as a function of the square of the output current in air and under vacuum.

amplitude-frequency coefficient can be defined as (Agarwal et al., 2006)

$$\kappa = \frac{\Delta f}{f_0}\frac{1}{I_d^2}, \tag{2.13}$$

where $\Delta f/f_0$ is the relative resonant frequency shift and I_d is the RMS drive current through the resonator. From Figure 2.6 the A-f coefficient was calculated in air and under vacuum to be -45 ppm/mA^2 and -12 ppm/mA^2, respectively (Filler, 1985).

As can be seen in Figure 2.7, the power-handling capability which corresponds to the critical vibration amplitude of the resonator was also characterized by measuring its 1-dB compression point (Shao et al., 2008; Kaajakari et al., 2004). The 1-dB compression points in air and under vacuum were measured to occur at available input powers of 5.29 dBm and -5.16 dBm. These are equivalent to a 0.32 mA and 0.14 mA RMS drive current in the resonator, respectively.

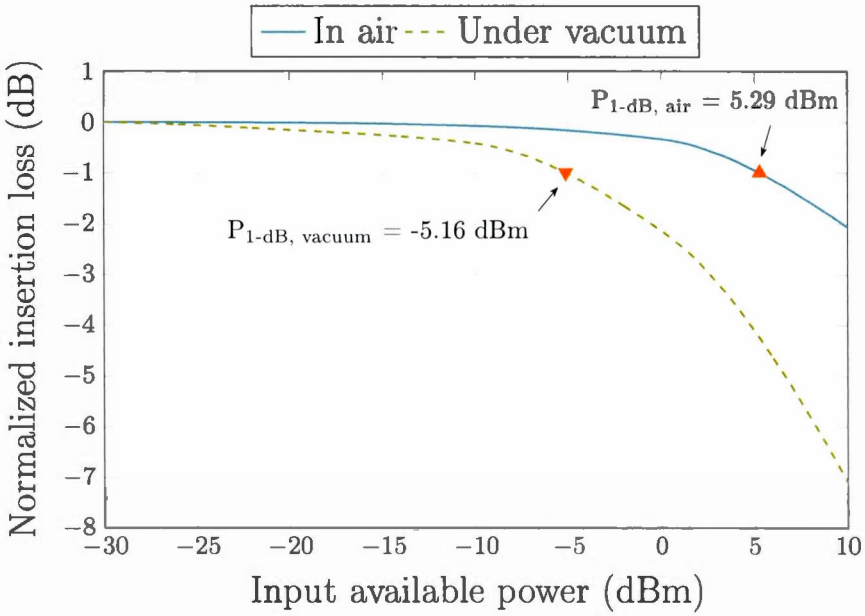


Figure 2.7: Measured resonator power-handling performance in air and under vacuum.

2.3.2 Transimpedance amplifier characterization

The fully differential TIA is fabricated in a TSMC 65 nm low-power process and consumes 1.4 mA from a 1-V supply. The circuit active area measures 150×220 μm^2, as shown in Figure 2.4. To obtain the frequency response of the TIA, S-parameters were measured using the Keysight E5061B VNA. The network analyzer input power level was set to -45 dBm and the S-parameters were taken from 100 kHz to 1 GHz. The transimpedance gain (Z_T) is calculated from the S-parameter characteristics as (Weiner et al., 2003)

$$Z_T = Z_0 \times \frac{S_{21}}{1 - S_{11}}, \tag{2.14}$$

where Z_0 represents the 50 Ω transmission line impedance.

Figure 2.8 shows the transimpedance gain and the 3−dB bandwidth of the TIA, versus two control signals, V_{CTRL_A} and V_{CTRL_BW}. The measured gain reaches ~81 dBΩ with bandwidth around 102 MHz extending to 214 MHz when the gain is reduced to

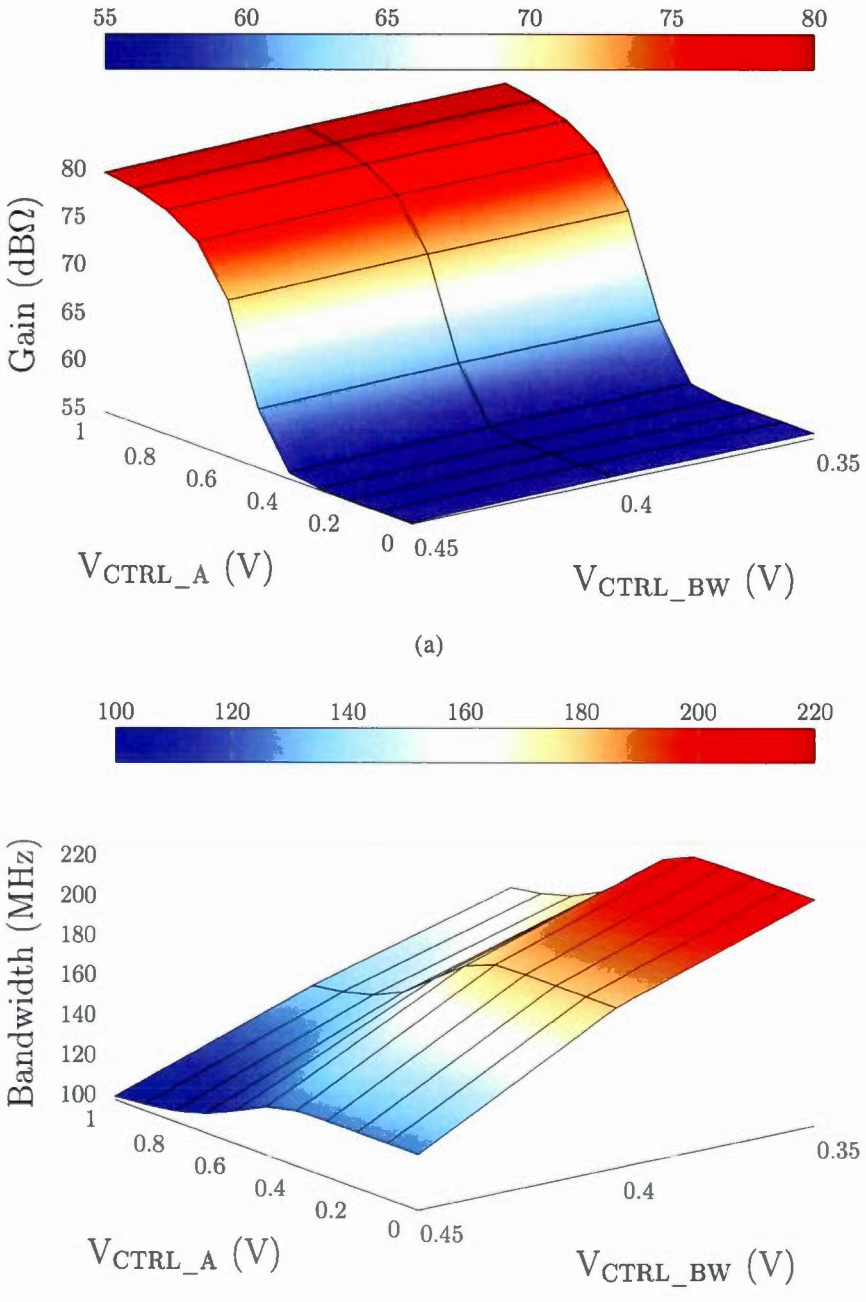


Figure 2.8: Measured TIA (a) transimpedance gain and (b) 3-dB bandwidth vs. V_{CTRL_A} and V_{CTRL_BW}.

55 dBΩ. Control voltages can be varied independently. Over the V_{CTRL_BW} range, the maximum gain variation for the same V_{CTRL_A} value is of ∼0.2 dB as seen in Figure 2.8(a). The worst case insertion loss extracted from Figure 2.5 (i.e., P_{in}=10 dBm in air) corresponds to a motional resistance equal to 1.7 kΩ which is corresponding to around 65 dBΩ. For an input power of −5 dBm the extracted motional resistance is equal to 1.35 kΩ which corresponds to 62.7 dBΩ. To overcome the resonator losses, the maximal transimpedance gain of the sustaining amplifier is fixed to 78 dBΩ and 170 MHz bandwidth which is amply sufficient to meet the oscillation conditions (discussed in section 2.3.3). The AGC loop can then reduce the gain once the oscillation has reached the appropriate amplitude. The magnitude of the input and output impedances of the TIA at the resonant frequency of the resonator are 81 Ω and 100 Ω, respectively.

Figure 2.9 shows the measured transimpedance gain at its maximum for different input power levels varying from −48 dBm to −20 dBm. A value of available power of −38.6 dBm was recorded for the 1-dB compression point of the TIA.

Figure 2.10 shows the input-referred current noise of the TIA measured with the Keysight N9030A spectrum analyzer across a 214 MHz bandwidth. At low frequencies, the noise is dominated by the flicker noise. The flat thermal noise floor is seen in the ∼20 kHz - 40 MHz frequency range, where the input-referred noise is below 4 pA/$\sqrt{\text{Hz}}$, then goes up with a f^2 slope because of the gain reduction beyond the bandwidth.

The performance parameters of the TIA configured at the 78 dBΩ gain-level are summarized in Table 2.2.

2.3.3 Oscillator characterization

2.3.3.1 Open-loop measurements

To confirm that sufficient loop gain was present for the oscillation, the resonator was connected to the TIA in open-loop configuration under vacuum, and the frequency and

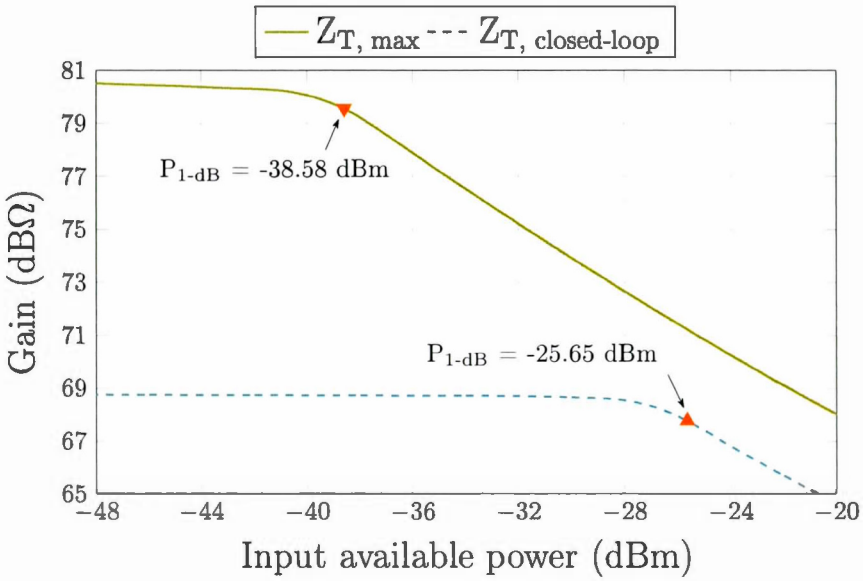


Figure 2.9: Measured 1-dB compression point of the TIA at the maximum transimpedance gain (solid line) and at the oscillation frequency in closed-loop configuration (dashed line).

Table 2.2: Performance parameters of the TIA (design 2).

Parameter	Measured value	
	TIA only	Closed-loop
Tranimpeande gain [dBΩ]	78	69
Bandwidth [MHz]	170	158
Input impedance, R_{in} @f_0 [Ω]	81	81
Output impedance, R_{out} @f_0 [Ω]	100	100
Power supply, V_{DD} [V]	1	1
Power Consumption, P_{DC} [mW]	1.4	1.4
Input-referred noise @f_0 $\left[pA/\sqrt{Hz}\right]$	3.65	10.4
1-dB compression point, $P_{1\text{-}dB}$ [dBm]	-38.6	-26.4
Active area [mm^2]	0.033	
Process	65 nm CMOS	

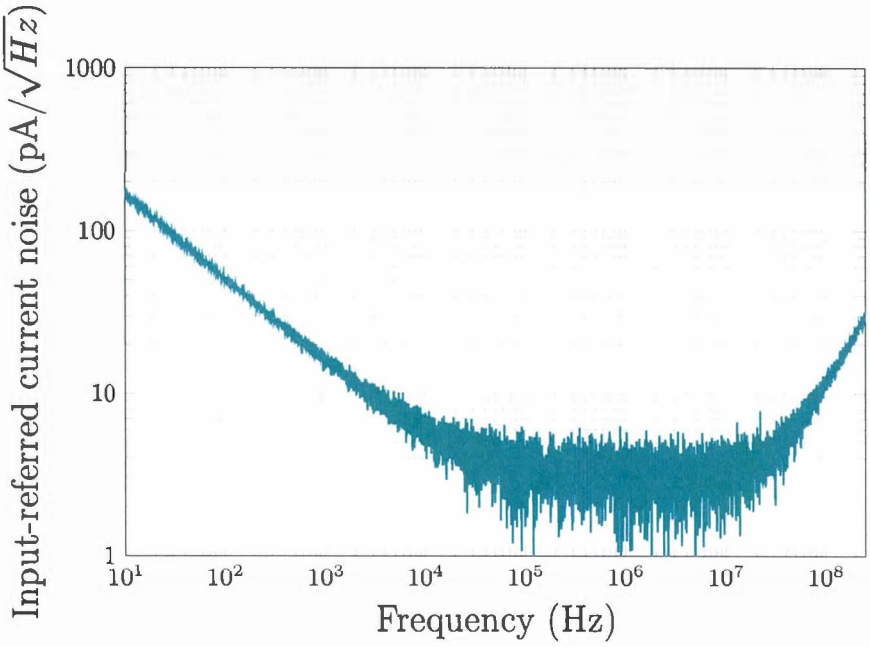


Figure 2.10: Measured input-referred current noise of the TIA.

phase responses were measured using the Keysight E5061B VNA. As illustrated in Figure 2.4 (dashed lines), the input and output ports of the VNA were connected to the differential inputs of the resonator and the differential outputs of TIA, respectively, through an external balun used to convert between differential and single-ended signals.

It is observed from Figure 2.11 that the open-loop gain at the resonant frequency of the resonator is higher than 0 dB as formulated in condition (1.15). Furthermore, phases measured for different V_{CTRL_BW} varying from 0.35 V to 0.45 V have variation $\Delta\phi$ of $\sim$40°. This variation is induced by tuning the bandwidth by means of V_{CTRL_BW} (Figure 2.8(b)). As a result, 0° phase shift was obtained for V_{CTRL_BW} = 0.38 V, satisfying condition (1.14). Accordingly, the main advantage of adjustable bandwidth feature is to set the oscillator total phase shift at open-loop configuration to 0° by setting the TIA phase shift ϕ_{TIA} to the suitable phase with regard to resonator phase shift ϕ_{MEMS}. This ensures that oscillation can be sustained in closed-loop. Therefore, the loaded Q-factor

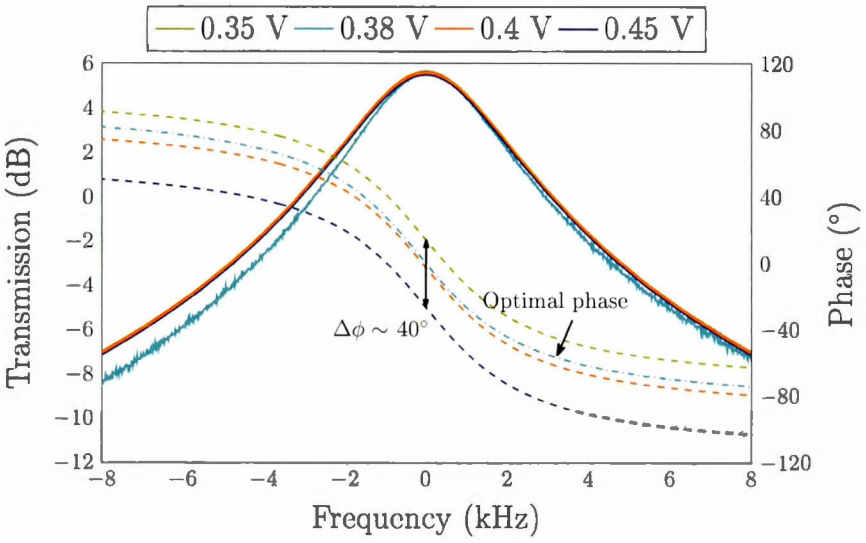


Figure 2.11: Measured open-loop gain and phase shift of the oscillator under vacuum.

was measured from the open-loop gain bandwidth to be of 4000.

2.3.3.2 Closed-loop measurements

The resonator and TIA were set in a closed-loop configuration (solid lines in Figure 2.4) and tested in air and under vacuum to characterize the performance of the oscillator. While operating in steady-state, the transimpedance gain at the oscillation frequency was set by the AGC loop control and the measured gain was recorded to be ~69 dBΩ with a 3-dB bandwidth of 158 MHz, as illustrated in Table 2.2. At this gain level, the input-referred 1-db compression point corresponded to −25.65 dBm, as shown in Figure 2.9. Using the Keysight N9030A spectrum analyzer, the output power of the oscillator, controlled by the AGC loop, was measured by probing the positive SSF output directly to the spectrum analyser, which was recorded to be −6 dBm, as shown in Figure 2.12. Therefore, the TIA remains in linear region so that can match the maximum drive power of the resonator which is below the TIA 1-dB compression capability.

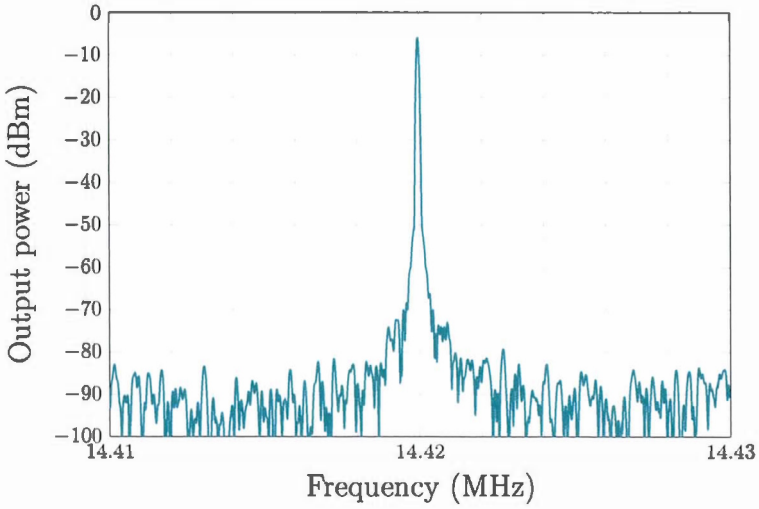


Figure 2.12: MEMS Oscillator output spectrum.

The expression for oscillator phase noise is given as follows (Hajimiri & Lee, 1998):

$$\mathcal{L}(f_m) = \frac{2FkT}{P_0} \times \left[1 + \left(\frac{f_0}{2Q_L f_m}\right)^2 \times \left(1 + \frac{f_c}{f_m}\right)\right], \tag{2.15}$$

where F represents the noise figure of the amplifier, P_0 is defined as the oscillation power, f_0 represents the carrier frequency, f_m the offset frequency from the carrier frequency, f_c is a constant related to $1/f$ noise corner of the oscillator and Q_L denotes the loaded Q-factor and is defined as

$$Q_L = Q_{UL} \times \frac{R_m}{R_m + R_{in} + R_{out}}, \tag{2.16}$$

where Q_{UL} is the intrinsic Q-factor of the resonator.

The phase noise measurements of the oscillator in air and under vacuum are plotted in Figure 2.13. The close-to-carrier phase noise was measured in atmospheric pressure and under vacuum to be -40 dBc/Hz and -60 dBc/Hz, respectively at a 10 Hz offset, and -104 dBc/Hz and -116 dBc/Hz, respectively at a 1 kHz offset. The phase noise floor reaches -130 dBc/Hz and is dominated by the TIA noise. The phase noise in the close-to-carrier region is improved by $\sim$20 dB under vacuum. This improvement is due

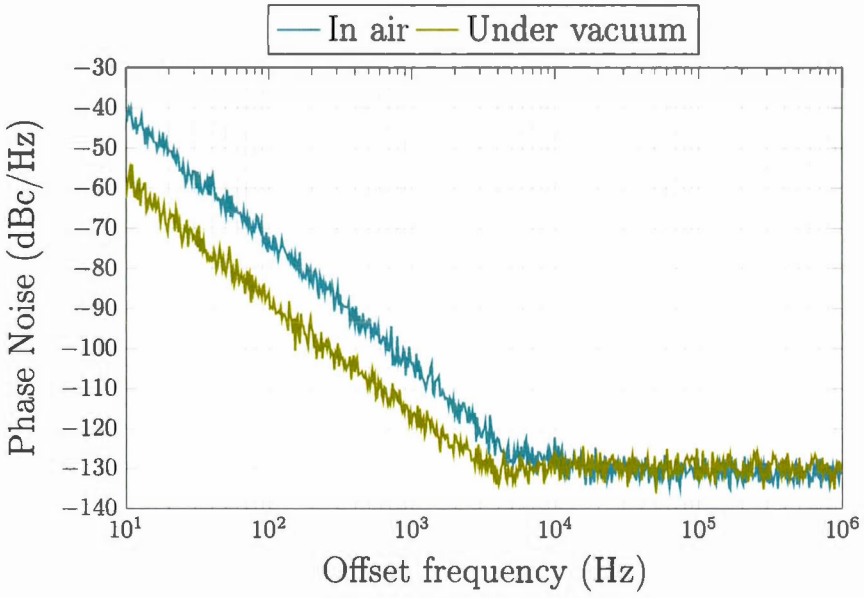


Figure 2.13: Measured phase noise of the MEMS-based oscillator in air and under vacuum.

to the considerable improvement in the loaded Q-factor, as expected from (2.15), which is caused by the higher resonator Q-factor, and the lower motional impedance R_m when operating under vacuum (Elsayed et al., 2016). On the other hand, the close-to-carrier phase noise follows the slope of $1/f^3$ which corresponds to the up-conversion of the flicker noise of the TIA. A $1/f^2$ region could not be observed as the flicker noise corner frequency is ~20 kHz (i.e., above the resonator's bandwidth). The fact that the close-to-carrier phase noise slope does not increase beyond $1/f^3$ indicates that the resonator and TIA non-linearities are not exerted. Otherwise, noise-folding could occur resulting in a slope larger than $1/f^3$ (Nabki & El-Gamal, 2008), deteriorating close-to-carrier phase noise performance.

Short-term stability is a key performance metrics of an oscillator and is a measure of its frequency stability. The measured frequency stability of the resonator is illustrated in Figure 2.14. The oscillator shows a broadening of the output frequency over a five-

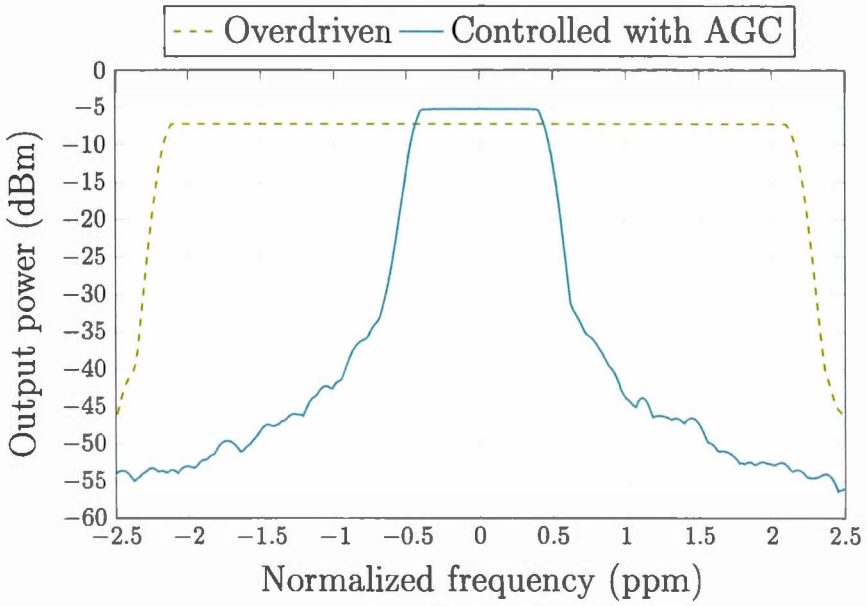


Figure 2.14: Oscillator signal short-time stability for the 14.42 MHz resonator (averaged over a five-minute time span) with and without the AGC loop.

minute time span. The frequency stability is improved from ±2.1 ppm to ±0.38 ppm, when the AGC is used, outlining the importance of not overdriving the resonator.

In order to obtain a representative comparison, a figure-of-merit (FOM) is used to compare the performance of the different oscillators in terms of phase noise and power consumption. It is given by (Zuo et al., 2010)

$$\text{FOM}_2 = \mathcal{L}(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_{\text{DC}}}{1\text{mW}}\right), \tag{2.17}$$

where P_{DC} is the DC power consumption of the oscillator circuit in mW. The calculated FOM values and summarized specifications for other published MEMS oscillators based on piezoelectric resonators are listed in Table 2.3. As can be seen, the MEMS oscillator demonstrated in this work has the best figure-of-merit $|\text{FOM}|$ when compared in air and under vacuum to other oscillators based on piezoelectric MEMS resonators (Pettine et al., 2012; Ruffieux et al., 2010; Zuo et al., 2010; Wu & Rais-Zadeh, 2015; Lavasani et al., 2012; Lavasani et al., 2015). Notably, the close-to-carrier

phase noise is lower under vacuum than the other works while dissipating relatively low-power consumption, thus offering a competitive phase noise at a 10 Hz offset. While the phase noise floor is higher than that of (Lavasani et al., 2012; Lavasani et al., 2015), the circuit operates at lower power. The phase noise floor could be improved by further reducing the noise of the TIA at the cost of increased power consumption. Moreover, the resonator could be driven at a higher power level at the cost of degraded close-to-carrier phase noise performance due to noise-folding. Finally, it is important to note that the resonator could be integrated in a system-in-package (SiP) in order to relax the design constraints of the TIA w.r.t. to gain-bandwidth, potentially yielding an enhanced FOM.

2.4 Conclusion

This chapter presented the design and implementation of a 14-MHz MEMS oscillator based on a piezoelectric disk resonator and a low-power high gain-bandwidth product fully differential transimpedance amplifier with adjustable bandwidth. The TIA was fabricated in a TSMC 65 nm CMOS process and consumes 1.4 mW. An input stage topology that is based on the RGC and CSFB topologies and characterized by a high gain, wide bandwidth and low input impedance was proposed. The TIA can reach a maximum gain of $\sim$80 dBΩ and features an adjustable bandwidth with a maximum of $\sim$214 MHz. The input-referred current noise floor of the TIA was measured to be below 3.7 pA/$\sqrt{Hz}$.

The presented MEMS oscillator achieves a measured phase noise in air and under vacuum of -104 dBc/Hz and -116 dBc/Hz at a 1-kHz offset, respectively, with a phase noise floor of -130 dBc/Hz. It also mitigates resonator and TIA non-linearities to attain a low close-to-carrier phase noise of -40 dBc/Hz and -60 dBc/Hz at a 10-Hz offset in air and vacuum, respectively. Its FOM relative to the state-of-the-art is superior because of its power consumption and close-to-carrier phase noise performance.

Table 2.3: Performance comparison of the proposed oscillator based on piezoelectric resonator with the state-of-the-art.

	(Pettine et al., 2012)	(Zuo et al., 2010)	(Wu & Rais-Zadeh, 2015)	(Lavasani et al., 2012)	(Lavasani et al., 2015)		This work	
CMOS technology	0.35 μm	0.5 μm	0.18 μm	0.18 μm	0.5 μm		65 nm	
Center frequency, f_0 [MHz]	2.17	222	78.6	427	35	175	14.42	
Testing condition	air	air	air	air	vacuum		air	vacuum
Quality factor, Q	450	2100	11601	1400	1800	3600	1952	4894
Motional resistance, R_m [kΩ]	80	0.035	0.058	0.18	1.36	0.26	1.2	0.9
AGC circuit	Yes	No	No	No	No		Yes	
Power supply, V_{DD} [V]	3.3	5	1.8	1.8	3		1	
Power consumption, P_{DC} [mW]	1.28	10	4.8	13	3.8	13.5	1.4	
Phase noise @10Hz [dBc/Hz]	-25	-22	-40	-10	-57	-48	-40	-60
Phase noise @1kHz [dBc/Hz]	-85	-88	-70	-82	-112	-103	-104	-116
Phase noise floor [dBc/Hz]	-105	-160	-122	-147	-142	-140	-130	-130
FOM_2 @10Hz [dB]	-121	-159	-171	-151	-182	-182	-162	-182
FOM_2 @1kHz [dB]	-151	-185	-161	-183	-197	-197	-186	-198

CHAPTER III

OSCILLATOR BASED ON CAPACITIVE RESONATOR

3.1 Lamé-mode MEMS resonator

A brief description of the Lamé-mode capacitive (i.e., electrostatic) MEMS resonator presented in (Elsayed & Nabki, 2017) is given in this section. Figure 3.1 illustrates exploded and assembled 3D renditions of the resonator structure. Structures were fabricated in a commercial silicon-on-insulator (SOI) technology, MicraGEM-Si, where they are realized through processing and wafer bonding of two SOI wafers (i.e., the top wafer and the bottom wafer). The top wafer has its handle layer removed after bonding to the bottom wafer such that the resonator is mainly composed of a single-crystalline silicon central square suspended structure acting as the Lamé bulk mode resonator. This suspended square is 30 μm thick, has a 230 μm side length, and is formed in the device layer of the top SOI wafer. The resonator square structure is anchored to the substrate through four suspension beams placed at the corner nodal points of the resonance mode. Pads for an electrical connection to the central square are present in the end of each suspension beam. This allows the connection of the DC polarization voltage required for the electrostatic actuation of the device. These support beams are patterned in the device layer of the top SOI wafer. The central structure is surrounded by four electrodes utilized for capacitive actuation and sensing of the structure. The electrodes are formed in the device layer of the top SOI wafer and are separated from the central square by a

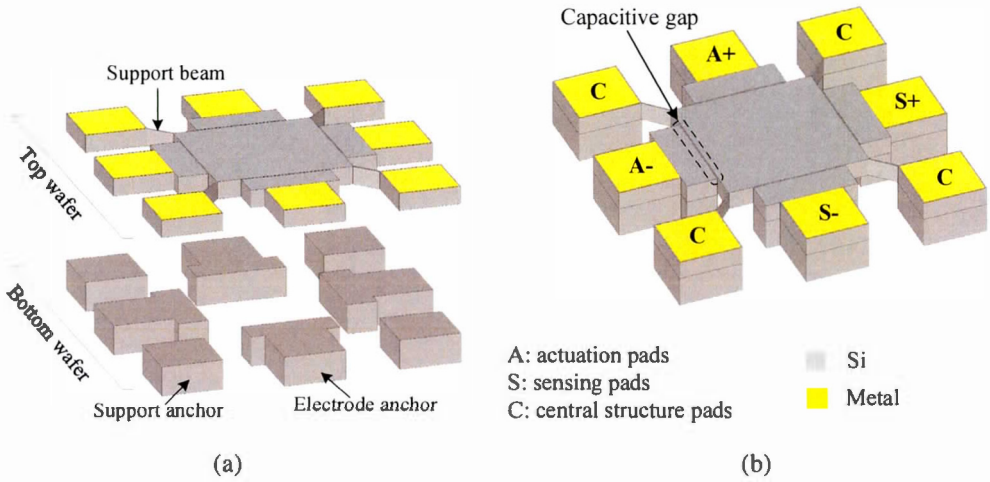


Figure 3.1: Simplified diagram of the (a) exploded and (b) assembled views of the Lamé-mode MEMS resonator with corner supports (Elsayed & Nabki, 2017).

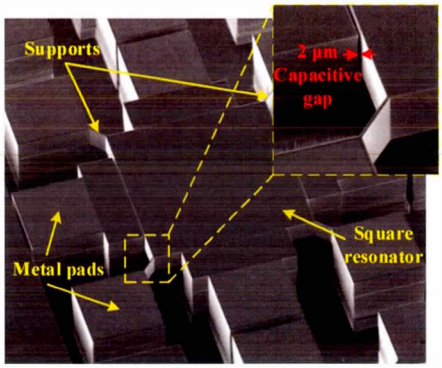


Figure 3.2: SEM micrograph of the Lamé-mode MEMS resonator with corner supports (Elsayed & Nabki, 2017).

2 μm capacitive transduction gap, which is the minimum spacing allowed by the technology. The device layer of the bottom SOI wafer is patterned to form the electrode anchors and the anchors at the end of the suspension beams. SEM micrographs of the resonator are shown in Figure 3.2. FEM simulations as well as theoretical calculations predict a resonance frequency of 17.9 MHz.

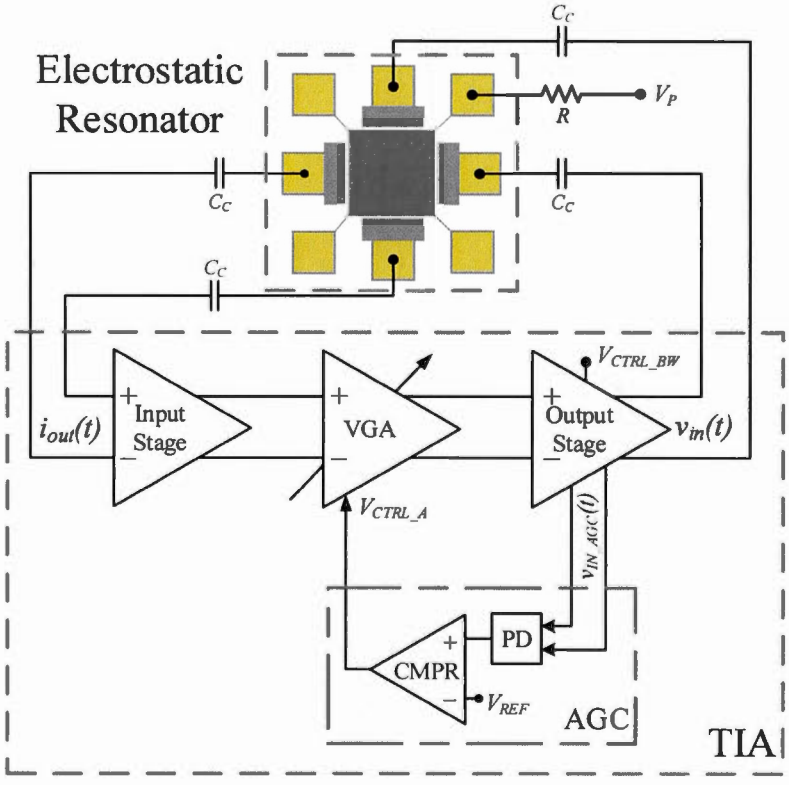
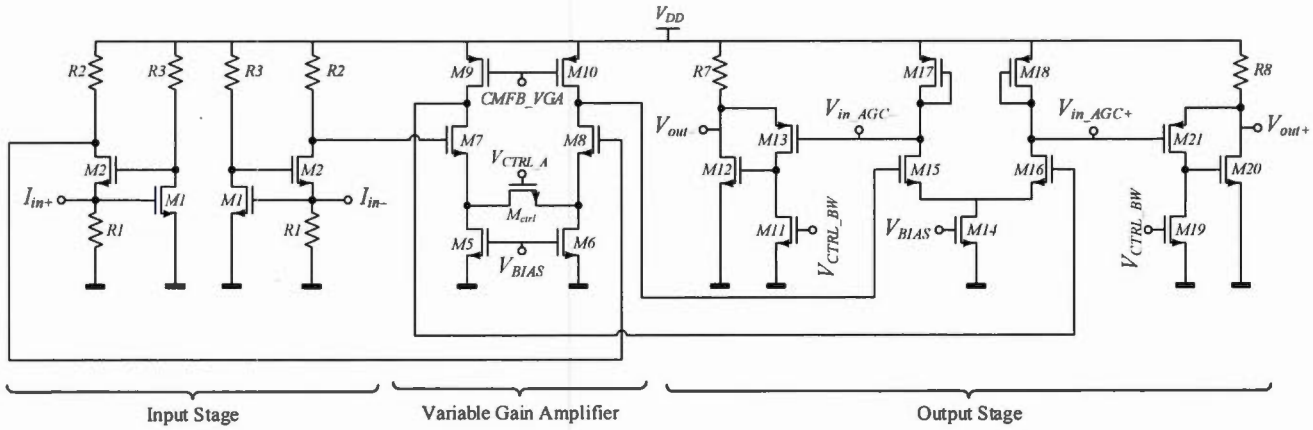


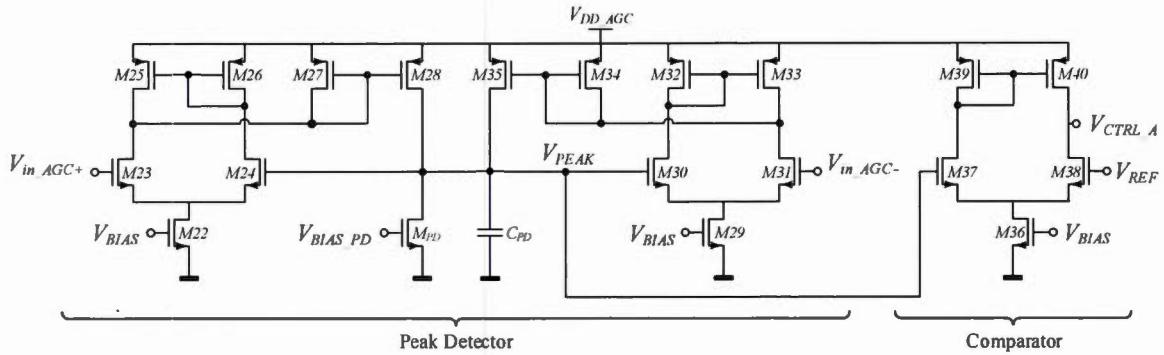
Figure 3.3: MEMS-Based oscillator functional diagram.

3.2 Transimpedance Amplifier Circuit Design

The TIA circuit shown in Figure 3.3 is composed of a three fully differential stages: *i*) an input stage followed by *ii*) a variable gain amplifier (VGA) controlled by an automatic gain control circuit (AGC), and *iii*) an output stage (super source follower (SSF)). The complete schematic circuit is shown in Figure 3.4 in which the biasing and common-mode feedback (CMFB) circuits are not shown. The sustaining amplifier provides low input impedance (R_{in}) and low output impedance (R_{out}) so as to compensate for large parasitic capacitance (C_P = 4 pF) and push the dominant pole far beyond the oscillation frequency. This translates into a high gain-bandwidth (GBW) product.



(a)



(b)

Figure 3.4: Circuit schematic of (a) the proposed fully differential TIA design, and (b) the AGC circuit.

The gain of the TIA needs to be high enough in order to compensate for the motional resistance of the MEMS resonator and sustain the oscillation. The regulated cascode (RGC) topology (Sackinger & Guggenbuhl, 1990) was chosen as input stage to achieve a reasonable trade-off between gain, bandwidth and power consumption.

The input impedance of the RGC input stage is given by

$$R_{in} = \frac{1}{g_{m2}\,(1 + R_3\,g_{m1})}, \tag{3.1}$$

where g_{m1} and g_{m2} are the transconductances of transistors $M1$ and $M2$, respectively. Thus, smaller input impedance can be attained by increasing voltage gain of the local feedback stage given by $(1 + R_3\,g_{m1})$.

The expression of input stage gain is given by

$$Z_T(s) \cong \frac{R_2\left(1 + s\dfrac{R_3C_1}{1 + R_3g_{m1}}\right)}{(1 + sR_1C_{in})\,(1 + sR_3C_1)\,(1 + sR_2C_{gd2})}, \tag{3.2}$$

where C_{in}, C_1, and C_{gd2} are the total input capacitances of the input stage, the equivalent capacitance between the drain of $M1$ and gate of $M2$, and the gate-drain capacitance of transistors $M2$, respectively. To achieve a higher gain, R_2 should be increased, although it cannot be arbitrarily enlarged because of design constraints.

It can be seen from (3.2) that the 3-dB bandwidth of the input stage is limited by the dominant pole appearing at the drain of transistor $M1$ and is given by

$$f_{-3dB} = \frac{1}{2\pi R_1C_{in}} \cong \frac{1}{2\pi R_1 \times (C_{gs1} + C_{gd1}R_3g_{m1})}, \tag{3.3}$$

where C_{gd1}, C_{gs1}, and C_{gs2} are the gate-drain capacitance of transistor $M1$, and the gate-source capacitances of transistors $M1$, and $M2$, respectively.

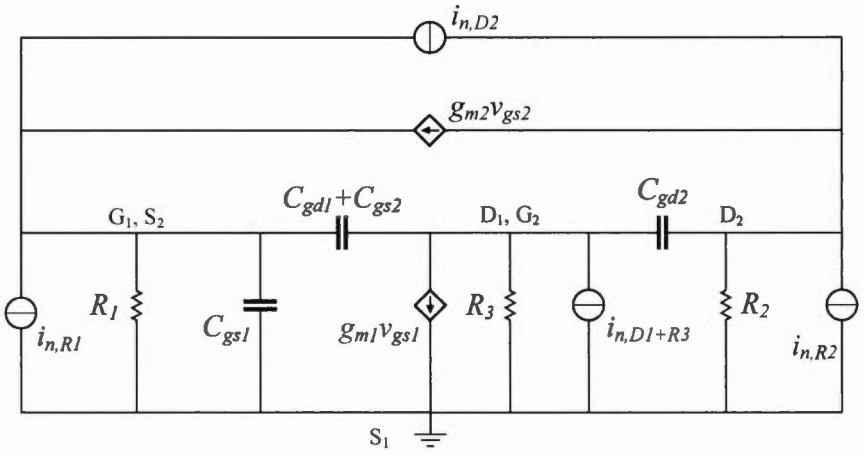


Figure 3.5: Simplified equivalent circuit of the RGC input stage used for noise analysis.

The local feedback of the input stage generates a zero at a frequency of

$$f_z \cong \frac{g_{m1}}{2\pi C_1} \cong \frac{g_{m1}}{2\pi \left[C_{gd1} + C_{gd2} \left(1 + \frac{R_2}{R_1} \right) \right]}. \tag{3.4}$$

To maintain the zero far away from the dominant pole (Park & Yoo, 2004), the gate-drain capacitance of transistor $M2$ should be reduced by decreasing its width. In this fashion, the RGC input impedance in (3.1) will not be dramatically affected since g_{m2} will not decrease considerably as it is proportional to $\sqrt{(W/L)_2}$, while its gate capacitance is linearly proportional to $(WL)_2$. This can be compensated by increasing R_3 as the input impedance is inversely proportional to $(1 + R_3\, g_{m1})$, as shown in (3.1).

The input-referred current noise is a key performance parameter to be considered when designing the proposed TIA. It can be used to provide a representative comparison between different circuit topologies. Since the noise is mostly contributed by the input stage, the noise of the other stages can be neglected. Therefore, a noise analysis carried-out using the equivalent circuit shown in Figure 3.5, and is based on the analysis method proposed in (Park & Yoo, 2004), where shot noise and flicker noise are neglected. Assuming that all noise sources are uncorrelated, the input-referred current noise of the

input stage can be shown to be given by

$$\overline{i_{n,in}^2} = \frac{4kT}{R_1} + \frac{\omega^2(C_1+C_2)^2}{g_{m2}^2}\left(\gamma g_{d0,2} + \frac{1}{R_2}\right) + \frac{4kT\left(\frac{1}{R_1^2} + \omega^2 C_{in}^2\right)}{\left(g_{m1} + \frac{1}{R_3}\right)^2}\left(\gamma g_{d0,1} + \frac{1}{R_3}\right), \tag{3.5}$$

where γ is the noise coefficient (Shaeffer & Lee, 1997; Ogawa, 1981), k is Boltzmann's constant, T is the absolute temperature, and $g_{d0,1}$ and $g_{d0,2}$ are the zero-bias drain conductance of transistors $M1$, and $M2$, respectively.

From (3.5), the noise can be analyzed as follows: the thermal noise contribution from R_1 is directly referred to the input, and as the frequency increases, the noise is dominated by terms containing ω^2. Therefore, a low input-referred noise can be achieved by increasing resistor R_1 and thus for better TIA performance in terms of noise.

3.3 Experimental Results

The resonator and the TIA were both characterized, and were then combined to implement the MEMS-based oscillator. Two test configuration setups shown in Figure 3.6 were used to characterize the MEMS-based oscillator: *i*) the open-loop configuration and *ii*) the closed-loop configuration.

3.3.1 Resonator Characterization

The frequency response of the resonator was measured in differential configuration with the VNA under a vacuum level of 100 mTorr for DC polarisation voltages, V_p, of 100 V and 200 V, and for various input power levels starting from -30 dBm up to 0 dBm. Figure 3.7 shows the transmission characteristic curves normalized to the center frequency of 17.93 MHz with a Q-factor of ~890k, and a peak transmissions of -57 dB and -45 dB for V_p = 100 V and V_p = 200 V, which correspond to motional

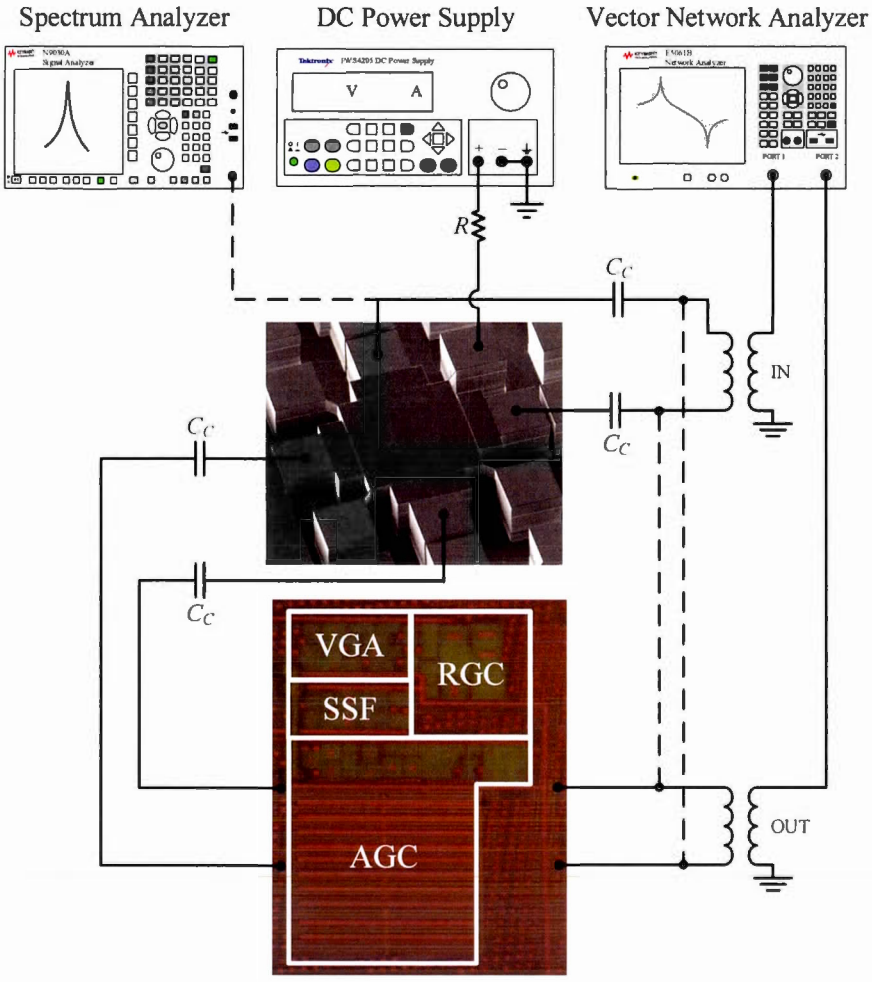
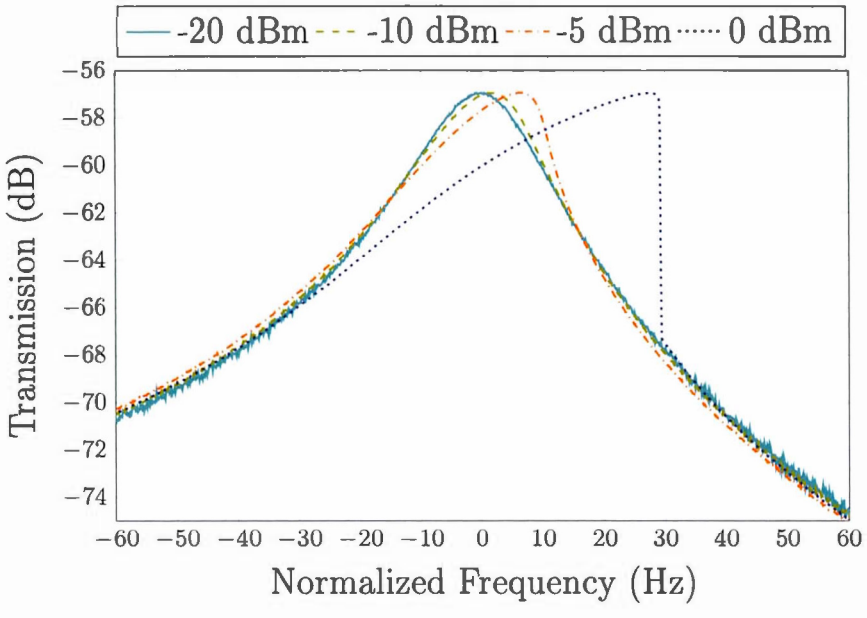
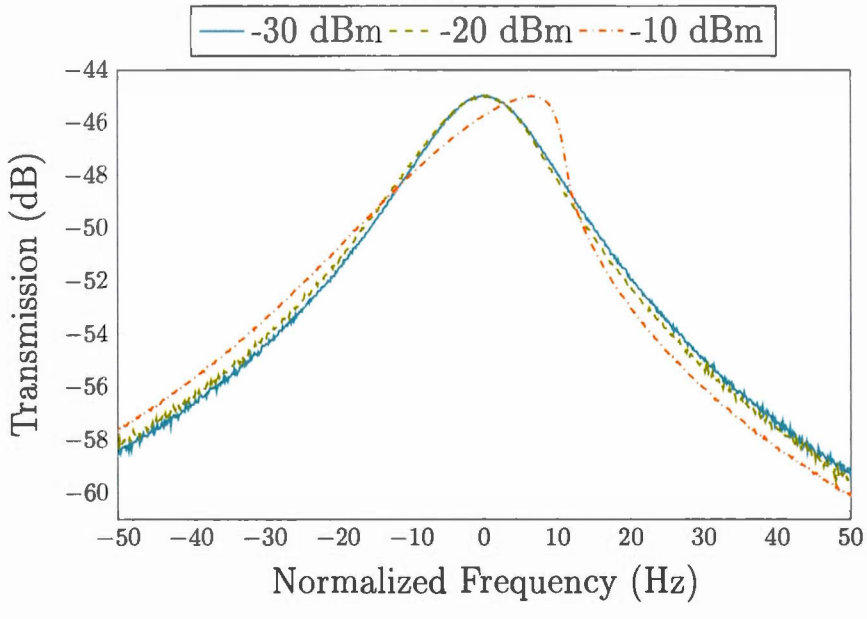


Figure 3.6: Test setup of the MEMS-based oscillator in open-loop (solid lines) and closed-loop (dashed lines) with micrographs of the TIA and resonator.

resistances of 35 kΩ and 8.8 kΩ, respectively. The results at high input power levels indicate spring-hardening non-linear behavior, as the Lamé-mode resonator geometry is aligned with the <100> crystalline silicon orientation (Zhu & Lee, 2014; Zhu & Lee, 2012; Zhu et al., 2012). Therefore, a positive amplitude–frequency (A–f) coefficient (κ) is associated with this resonator (Bouchami & Nabki, 2014).



(a)



(b)

Figure 3.7: Normalized resonator transmission characteristic curves for various output input amplitude levels for (a) V_p = 100 V and (b) V_p = 200 V.

3.3.2 Transimpedance Amplifier Characterization

The fully differential TIA is fabricated in a 65 nm CMOS process from TSMC, and consumes only 0.9 mA from a 1-V supply. The total circuit area measures 130×225 μm^2, as shown in Figure 3.6. To obtain the frequency response of the TIA, S-parameters were measured using a Keysight E5061B VNA in a frequency range from 100 kHz to 1 GHz with an input power level of -45 dBm.

Figure 3.8 shows the transimpedance gain and the 3-dB bandwidth of the TIA, versus two control signals, V_{CTRL_A} and V_{CTRL_BW}. The maximum achievable gain is 98 dBΩ with a bandwidth of 90 MHz. The bandwidth can be extended to 142 MHz when the gain is reduced to 83 dBΩ. Control voltages can be varied independently in such a way that the gain and bandwidth are also independent from each other. As such, as V_{CTRL_BW} varies from 0.35 V to 0.45 V, the maximum gain variation (for the same V_{CTRL_A} value) is $\sim$0.32 dB (as seen in Figure 3.8(a)). The motional resistances of 35 kΩ and 8.8 kΩ, extracted from Figure 3.7 for V_p of 100 V and 200 V, respectively, correspond to 91 dBΩ and 79 dBΩ, respectively, which can be covered by the maximum gain available of the proposed TIA to ensure sufficient gain for oscillation.

Figure 3.9 shows the input-referred current noise of the TIA measured with a Keysight N9030A spectrum analyzer across a 142 MHz bandwidth. At low frequencies, the noise is dominated by the flicker noise, while the input current noise spectrum is flat in the frequency range from $\sim$500 kHz to 142 MHz where the input-referred noise is dominated by the white noise and reaches 15 pA/$\sqrt{Hz}$.

Figure 3.10 shows the measured transimpedance gain for different input power levels varying from -50 dBm to -35 dBm. The TIA 1-dB compression point was extracted to be of -39 dBm. The performance parameters of the TIA are summarized in Table 3.1.

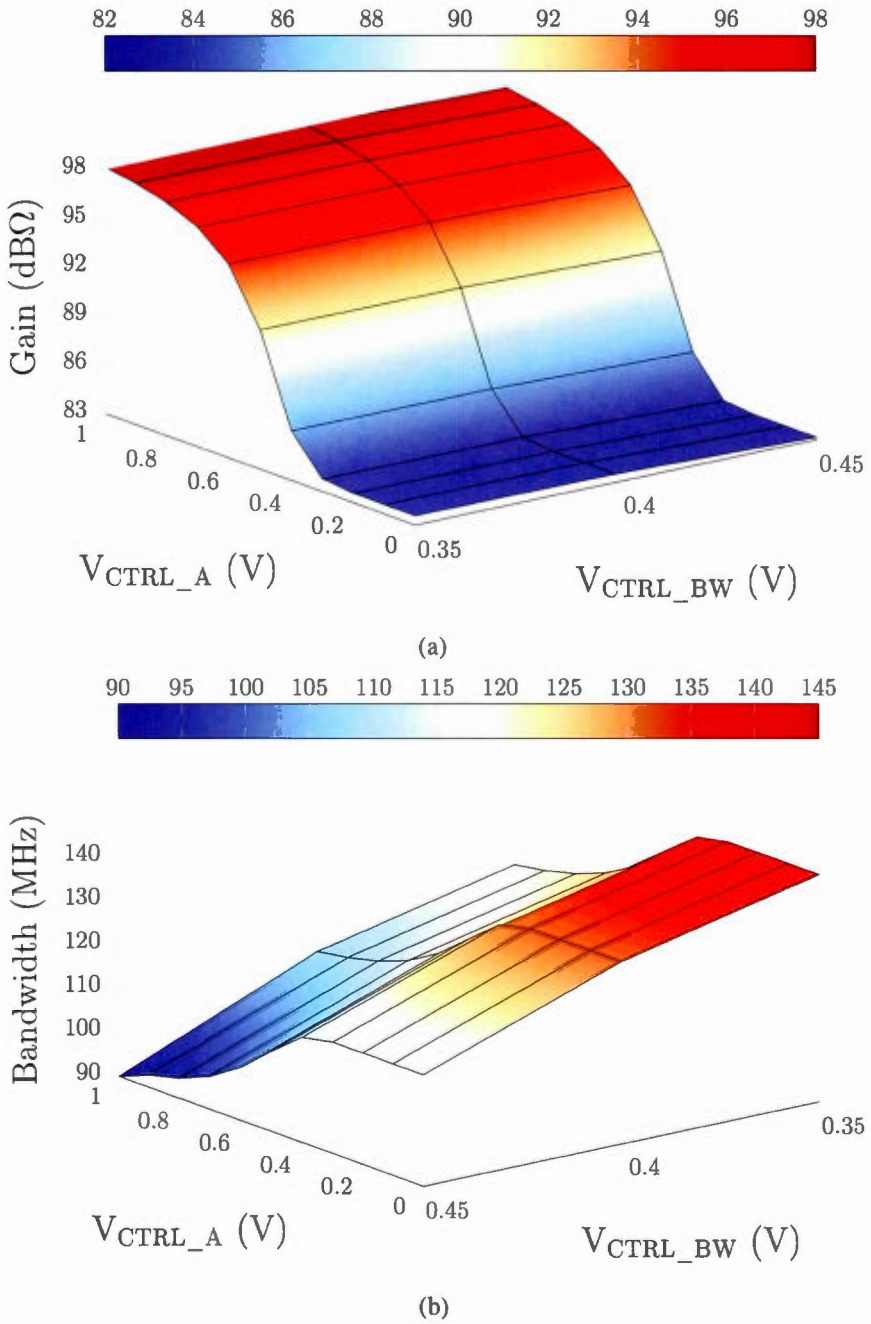


Figure 3.8: Measured TIA (a) gain and (b) bandwidth for different values of V_{CTRL_A} and V_{CTRL_BW}.

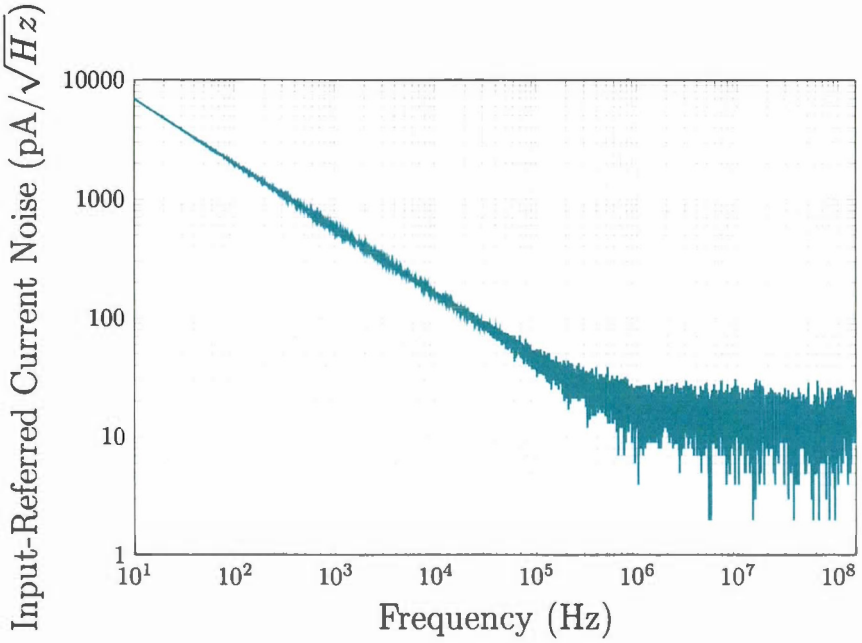


Figure 3.9: Measured TIA input-referred current noise.

Table 3.1: Performance parameters of the TIA (design 1).

Parameter	Measured Value
Tranimpeande gain [dBΩ]	98
Bandwidth [MHz]	170
Input impedance, R_{in} @ f_0 [Ω]	89
Output impedance, R_{out} @ f_0 [Ω]	100
Power supply, V_{DD} [V]	1
Power Consumption, P_{DC} [mW]	0.9
Input-referred noise @f_0 $\left[pA/\sqrt{Hz}\right]$	14.5
Total circuit area [mm^2]	0.029
Process	65 nm CMOS

3.3.3 MEMS Oscillator Characterization

3.3.3.1 Open-loop measurements

To confirm that sufficient loop gain was present for the oscillation, the resonator was connected to the TIA in open-loop configuration under vacuum, and the frequency and

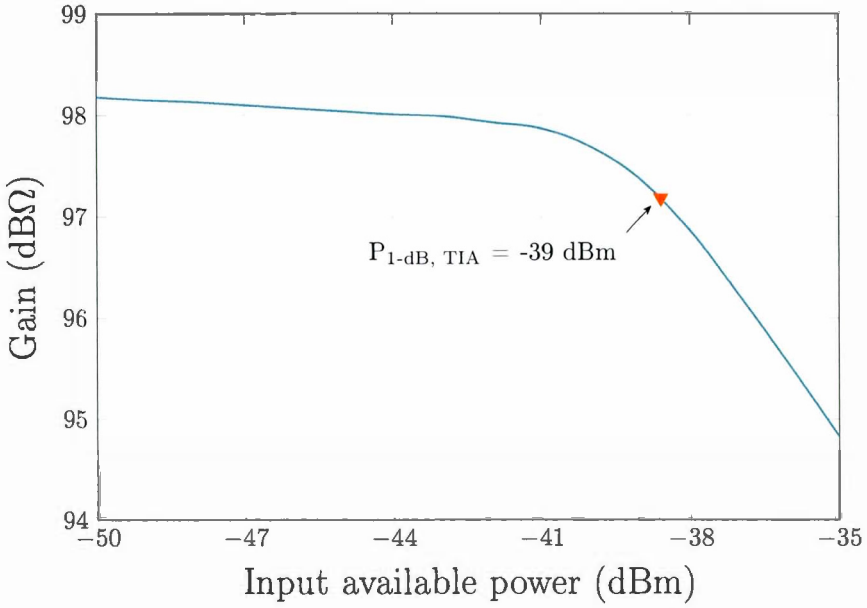


Figure 3.10: Measured TIA gain for different input power levels, outlining the 1-dB compression point.

phase responses were measured using a Keysight E5061B VNA. As illustrated in Figure 3.6, the input and output ports of the VNA were connected to the differential inputs of the resonator and the differential outputs of the TIA, respectively, through external baluns which are used to convert between single-ended and differential signals.

It is observed from Figure 3.12 that the open-loop gain and phase shift at the resonant frequency of the resonator is higher than 0 dB and equal to 0°, respectively, as formulated in conditions (1.14) and (1.15), thus ensuring that oscillation could be sustained in closed-loop. In addition, the loaded Q-factor was measured from the open-loop gain bandwidth to be around 875,000.

3.3.3.2 Closed-loop measurements

The resonator and TIA were set in a closed-loop configuration (dashed lines in Figure 3.6) and tested under vacuum to characterize the performance of the oscillator.

The phase noise measurements of the oscillator under vacuum are plotted in Figure 3.11 for polarization voltages of 100 V and 200 V. The near-carrier phase noise at a 10 Hz offset was measured to be approximately of -50 dBc/Hz and of -70 dBc/Hz at polarization voltages of 100 V and 200 V, respectively. At an offset of 1 kHz, the phase noise was measured to be of -120 dBc/Hz at both polarization voltages. At a polarization voltage of 100 V, the the TIA flicker noise dominates the close-to-carrier phase noise. However, at a polarization voltage of 200 V, the close-to-carrier phase noise is deteriorated by the resonator non-linearity (Li et al., 2015). This results in the phase noise in the close-to-carrier region to be improved by $\sim$20 dB when V_p is decreased. At farther frequency offsets, the phase noise reaches a floor of -127 dBc/Hz and is dominated by the TIA noise.

These phase noise measurements translate in time-domain jitter values. The RMS integrated phase jitter (from 12 kHz to 20 MHz) is equal to 14 ps. Short-term stability is an importance performance criteria of the oscillator and is a measure of its frequency stability. The frequency stability of the resonator is illustrated in Figure 3.13. The oscillator shows a broadening of the frequency output over a five-minute time-span. Note that the frequency stability is improved when the AGC is used, from ± 1.04 ppm to ± 0.25 ppm, as this ensures that the non-linearity of the resonator is not exerted.

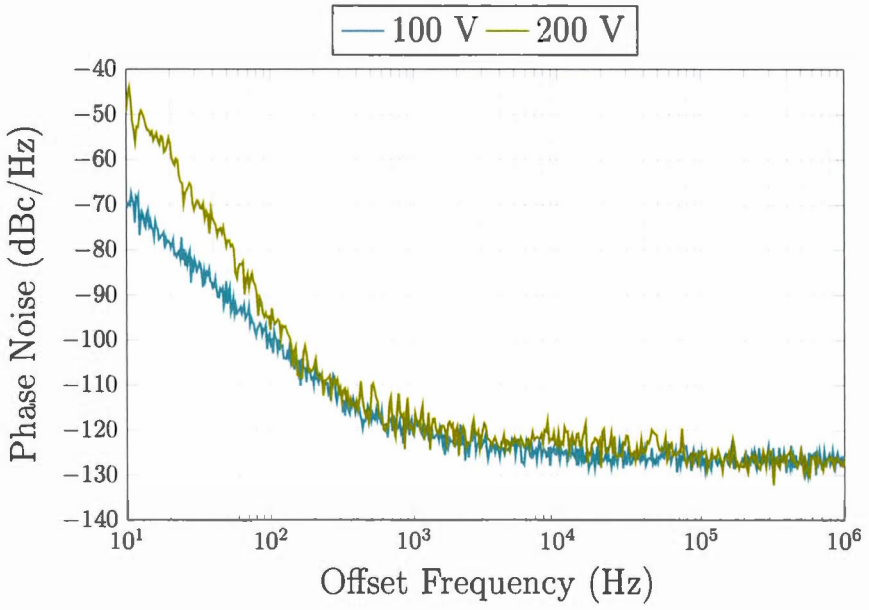


Figure 3.11: Measured phase noise in vacuum for polarization voltages of 100 V and 200 V.

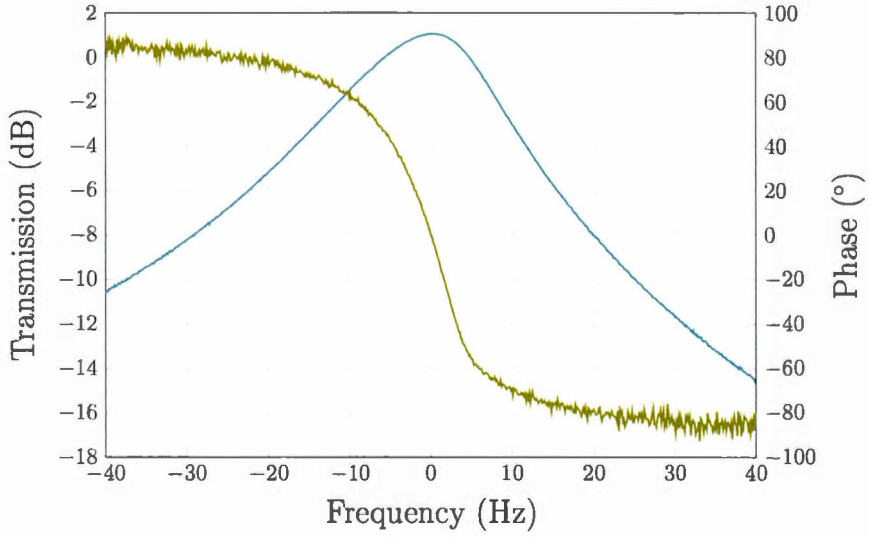


Figure 3.12: Measured open-loop gain and phase shift of the oscillator loop under vacuum at V_p = 100 V.

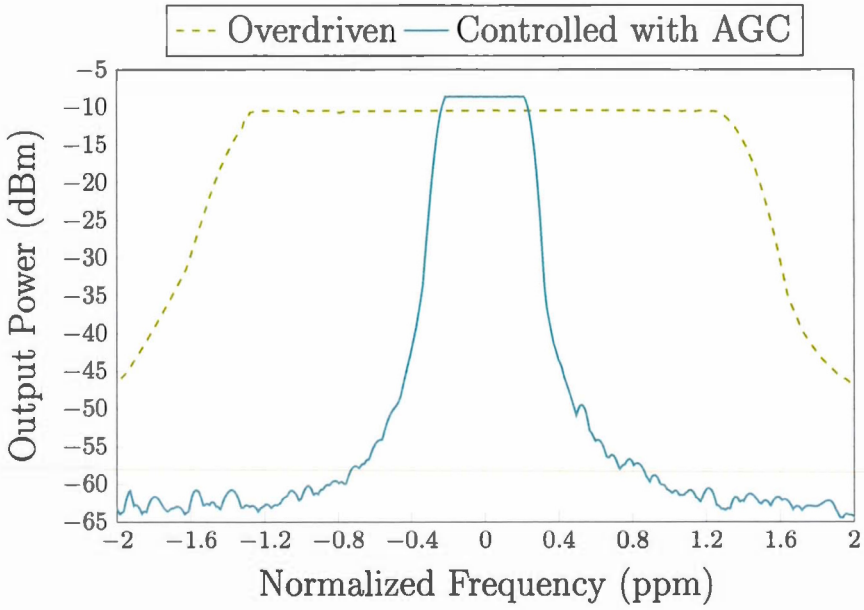


Figure 3.13: MEMS oscillator signal short time stability at a 17.93 MHz central frequency (averaged over a five minute time span) with V_p = 100 V.

Table 3.2: Performance comparison of the proposed oscillator based on capacitive resonator with the state-of-the-art.

	(Seth et al., 2012)	(Lin et al., 2004b)	(Sundaresan et al., 2006)	(Chen et al., 2013)	(Li et al., 2015)	(Huang et al., 2008)	This Work
CMOS technology	0.35 μm	0.35 μm	0.18 μm	0.18 μm	0.35 μm	0.35 μm	65 nm
Gap [nm]	1500	80	200	50	600	100	2000
Center frequency, f_0 [MHz]	20	61.2	103	18	1.18	10.92	17.93
Testing condition	vacuum	air	air	vacuum	vacuum	vacuum	vacuum
Quality factor, Q	160,000	48,000	80,000	8,000	3,029	1,092	889,539
Motional resistance, R_m [kΩ]	65	1.5	5	76.9	700	6	20
Polarisation voltage, V_p [V]	26	12	18	2.5	45	5	100
AGC Circuit	Yes	No	Yes	No	Yes	No	Yes
Power supply, V_{DD} [V]	2.5	3.3	1.8	1.8	2.5	3.3	1
Power consumption, P_{DC} [mW]	6.9	0.95	2.6	5.9	1.3	0.35	0.9
PN @1kHz [dBc/Hz]	-105	-100	-108	-116	-112	-80	-120
PN Floor [dBc/Hz]	-131	-130	-136	-130	-120	-96	-127
FOM_2 @1kHz [dB]	-183	-196	-204	-193	-172	-165	-205
FOM_3 [$Hz^2\Omega^2$]	3.6×10^{17}	1.7×10^{19}	1.3×10^{19}	2.2×10^{18}	1.2×10^{19}	1.9×10^{14}	3.8×10^{19}

To allow for a representative comparison, two figure-of-merits FOM_2 (see (2.17)), and FOM_3, are used to evaluate the overall MEMS oscillator performance in terms of 1) phase noise and power consumption, and 2) phase noise floor and motional resistance. The expression of FOM_3 is given by (Seth et al., 2012)

$$\text{FOM}_3 = \frac{kT}{\text{PN Floor} \times P_{DC}} f_0^2 R_m^2, \tag{3.6}$$

It can be noticed that proposed FOM_3 is used to evaluate the low phase noise enabled by the TIA while considering the high resonator motional resistance (Seth et al., 2012). The calculated FOM_2 and FOM_3 values for different MEMS oscillators based on electrostatic resonators in the literature are listed in Table 3.2. As can be seen, the MEMS-based oscillator demonstrated in this work has the best figure-of-merits $\left|\text{FOM}_2\right|$ and FOM_3 when compared to others (Seth et al., 2012; Lin et al., 2004b; Sundaresan et al., 2006; Chen et al., 2013; Li et al., 2015; Huang et al., 2008) illustrating the performance of the proposed oscillator. Its close-to-carrier phase noise is notably lower as a result of the low noise of the TIA and the mitigation of the resonator non-linearity.

3.4 Conclusion

This paper presented a MEMS oscillator based on a Lamé-mode capacitive MEMS resonator and a fully differential high gain TIA. The TIA was fabricated in a 65 nm CMOS process from TSMC and consumes 0.9 mW from a 1-V supply. An RGC input stage was used in this work to benefit from high gain, wide bandwidth and lower input impedance which make it suitable for oscillators based on capacitive MEMS resonators. The TIA can reach a maximum gain of around 98 dBΩ and has an adjustable bandwidth with a maximum bandwidth of around 142 MHz. The input-referred current noise of the TIA was measured below 15 pA/$\sqrt{Hz}$ in the mid-band.

The proposed TIA was integrated with an 18-MHz Lamé-mode MEMS resonator to implement an oscillator. The presented MEMS oscillator achieves a phase noise of

-120 dBc/Hz, at a 1-kHz offset and the phase noise floor is of -127 dBc/Hz. The oscillator exhibits a superior figure-of-merit relative to the state-of-the-art in terms of power consumption and phase noise.

CONCLUSION

In this thesis, the realization of CMOS transimpedance amplifier capable to interface with series-resonant MEMS oscillator applications was studied. First, a Verilog-A model for a clamped-clamped beam resonator was presented where electrical and mechanical non-linear effects were exposed. Moreover a transimpedance amplifier designed in 0.13 μm CMOS was implemented with the model and MEMS-based oscillator simulation performances were done. The main goal of this work was to design two micromechanical reference oscillators based on both piezoelectric and capacitive MEMS resonators. The MEMS resonators presented here were developed in previous works (Elsayed & Nabki, 2017; Elsayed et al., 2016). Moreover, two transimpedance amplifier designs were studied in details in which frequency and noise analyses were developed for tradeoff condiseration. The first design was interfaced with the Lamé-mode capacitive resonator (Elsayed & Nabki, 2017). This design was characterized with higher gain in order to compensate resonator's losses, thereby sustaining oscillation. A regulated cascode (RGC) topology was used as an input stage to benefit from high gain with lower input stage and power consumption. The second transimpedance amplifier was interfaced with bulk-mode disk piezoelectric resonator (Elsayed et al., 2016). This design had a lower gain since the motional resistance of piezoelectric resonators is low. The input stage of the second design was based on RGC topology mixing with common source active feedback advantage topology in which lower input-referred current noise and larger bandwidth were achieved. The architecture of transimpedance amplifiers was fully differential and was characterized with an adjustable gain and bandwidth separately feature. Finally, the measured performances of MEMS-based oscillators were demonstrated and compared with state-of-the-art oscillators. Proposed MEMS-based

oscillators offered superior figure-of-merit in terms of power consumption and phase noise.

Future research will be focused on modeling Lamé-mode and disk resonators for further non-linearity effect consideration. Also MEMS switch will be used in MEMS-based oscillator to select from multiple resonators interfaced with the TIA in one single chip.

APPENDIX A

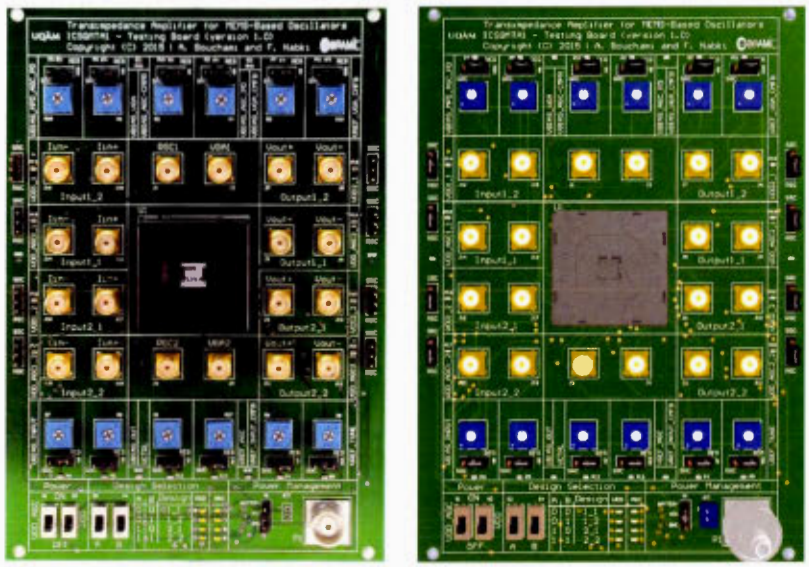
CMOS CHIP AND CHARACTERIZATION EVALUATION TEST BOARD

A.1 Printed circuit evaluation board

A Printed circuit board (PCB) was designed in order to characterize the transimpedance amplifiers. The double sided PCB shown in Figure A.1 and Figure A.2 was made with a standard 0.062 in ($\sim$1.5 mm) glass-reinforced FR-4 epoxy laminate and the final dimension was 10×15 cm^2. The different power supplies are provided from off-chip low dropout (LDO) voltage linear regulators where their input power supplies are generated through one source path with available option of concocting to an external DC power supply or $3\times$AAA batteries.

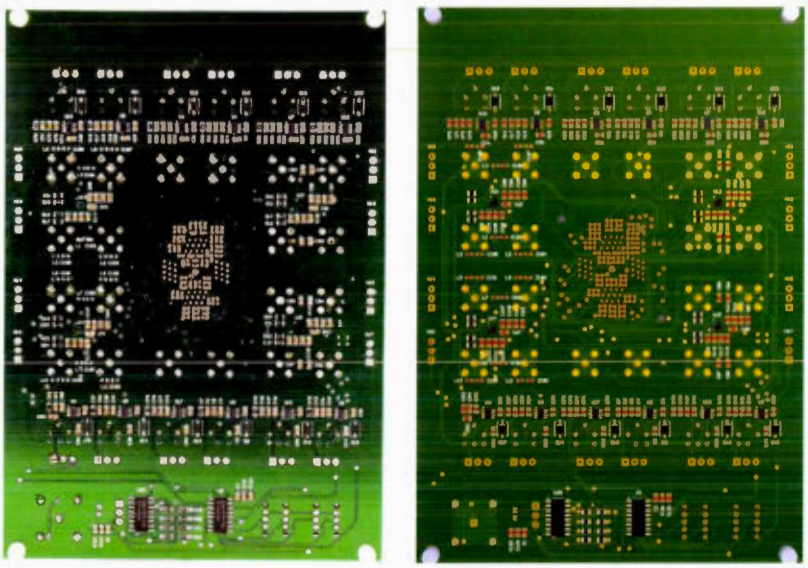
A.2 CMOS Transimpedance amplifier chip

A 48-pin QFN socket was used to place available CMOS chip packages for easier use. The micrograph of CMOS chip die is provided in Figure A.3 where TIAs were fabricated using TSMC 65 nm process. The die has 48 pins with dimension of 1.5×0.7 mm^2 and contains two main different designs for transimpedance amplifier. Each design was cloned in such a way for both designs, every TIA's stage has an external pin connection. It is noted that every design has a separate power supply pad. Thus, the design is selected through PCB using two slide switchers. Finally, the 48-QFN functional diagram package is shown in Figure A.4 and the pad description is illustrated in Table A.1.



(a) (b)

Figure A.1: Evaluation board (a) photograph and (b) 3D top view.



(a) (b)

Figure A.2: Evaluation board (a) photograph and (b) 3D bottom view.

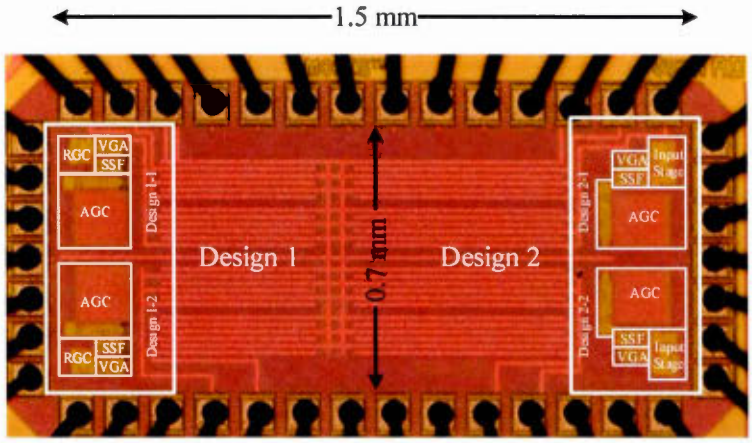


Figure A.3: Micrograph of complete transimpedance amplifier die fabricated in 65 nm CMOS process.

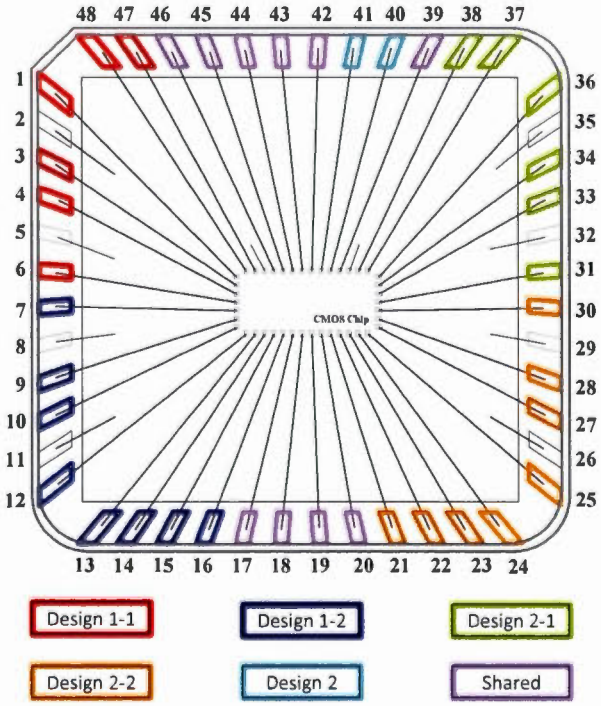


Figure A.4: Chip package pad layout functional diagram.

Table A.1: Chip package pad description.

Pin No.	Pin name	Pin type	Design consideration	Description
1	IN1_1+	Analog input	Design 1-1	Positive current input
2	VSS	Power	Shared	Ground
3	IN1_1-	Analog input	Design 1-1	Negative current input
4	OUT1_1+	Analog output	Design 1-1	Positive voltage output
5	VSS	Power	Shared	Ground
6	OUT1_1-	Analog output	Design 1-1	Negative voltage output
7	OUT1_2+	Analog output	Design 1-2	Positive voltage output
8	VSS	Power	Shared	Ground
9	OUT1_2-	Analog output	Design 1-2	Negative voltage output
10	IN1_2-	Analog input	Design 1-2	Negative current input
11	VSS	Power	Shared	Ground
12	IN1_2+	Analog input	Design 1-2	Positive current input
13	Input_Stage1	Analog I/O	Design 1-2	Input stage positive voltage output
14	VGA1	Analog I/O	Design 1-2	VGA positive voltage output
15	VDD1_2	Power	Design 1-2	1-V power supply

Pin No.	Pin name	Pin type	Design consideration	Description
16	VDD_AGC1_2	Power	Design 1-2	AGC 1-V power supply
17	VBIAS_AGC_CMPR	Biasing	Shared	Comparator Bias voltage
18	VBIAS_AGC_PD	Biasing	Shared	Peak detector bias voltage
19	VBIAS_MPD_AGC_PD	Biasing	Shared	current source bias voltage
20	VREF_AGC	Reference	Shared	Comparator reference voltage
21	VDD_AGC2_2	Power	Design 2-2	AGC 1-V power supply
22	VDD2_2	Power	Design 2-2	1-V power supply
23	VGA2	Analog I/O	Design 2-2	VGA positive voltage output
24	Input_Stage2	Analog I/O	Design 2-2	Input stage positive voltage output
25	OUT2_2+	Analog output	Design 2-2	Positive voltage output
26	VSS	Power	Shared	Ground
27	OUT2_2-	Analog output	Design 2-2	Negative voltage output
28	IN2_2-	Analog input	Design 2-2	Negative current input
29	VSS	Power	Shared	Ground
30	IN2_2+	Analog input	Design 2-2	Positive current input
31	OUT2_1-	Analog output	Design 2-1	Negative voltage output
32	VSS	Power	Shared	Ground

Pin No.	Pin name	Pin type	Design consideration	Description
33	OUT2_1+	Analog output	Design 2-1	Positive voltage output
34	IN2_1+	Analog input	Design 2-1	Positive current input
35	VSS	Power	Shared	Ground
36	IN2_1-	Analog input	Design 2-1	Negative current input
37	VDD2_1	Power	Design 2-1	1-V power supply
38	VDD_AGC2_1	Power	Design 2-1	AGC 1-V power supply
39	VCTRL_BW	Analog input	Shared	Adjust bandwith
40	VREF_INPUT_CMFB	Reference	Design 2	Input Stage CMFB reference voltage
41	VBIAS_INPUT	Biasing	Design 2	Input Stage CMFB bias voltage
42	VBIAS_OUT	Biasing	Shared	output stage bias voltage
43	VCTRL_A	Control	Shared	VGA gain manual control
44	VREF_VGA_CMFB	Reference	Shared	VGA CMFB reference voltage
45	VBIAS_VGA_CMFB	Biasing	Shared	VGA CMFB bias voltage
46	VBIAS_VGA	Biasing	Shared	VGA bias voltage
47	VDD_AGC1_1	Power	Design 1-1	AGC 1-V power Supply
48	VDD1_1	Power	Design 1-1	1-V power supply

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